Tb/s Switching Fabrics for Optical Interconnects Using Heterointegration of Plasmonics and Silicon Photonics: The FP7 PLATON Approach

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Abstract We present recent work that is carried out within the FP7 project PLATON on novel Tb/s switch fabric architectures and technologies for optical interconnect applications, employing heterointegration of plasmonics, silicon photonics and electronics.

Introduction

Size and power consumption appear to be daunting issues in today's Peta-flop High-Performance Computing (HPC) machines [1], indicating that new architectural and technological considerations will be required in order to be able to move towards Exa-scale computing powers. Servers and network switches are already consolidating into high-density blade enclosures in order to reduce space and cooling requirements [2], whereas silicon photonics emerges as a powerful technology for low-loss and high-bandwidth optical connectivity in integrated circuit environments [3]. This roadmap raises, however, new challenges for the switching infrastructures of miniature data networks: next-generation routing circuitry has to provide high throughput capabilities while keeping in-line with the requirements of small foot-print, low latency and low power consumption.

In this article, we demonstrate recent work performed within the frame of the FP7 project PLATON targeting the deployment of Tb/s routing fabrics for optical interconnect applications. We present a 4x4 router platform that relies on a novel integration concept promoting the use of innovative thermo-optic Dielectric-Loaded Surface Plasmon Polariton (DLSPP) switches [4-6] integrated with Silicon-on-Insulator (SOI) passive photonic components and electronic processing circuitry. Preliminary simulation results of a 4:1, 100GHz channel spacing SOI multiplexer and of a 2x2 DLSPP switching element are presented, concluding with their combined utilization towards 2x2 routing of 320Gb/s aggregate optical traffic.

PLATON's Tb/s Silicon-Plasmonic Router

Fig. 1(a) shows the block diagram of our 4x4 router platform architecture. It exploits a SOI motherboard employing 340x400nm^2 waveguide structures and hosting four 7:1 SOI multiplexing circuits, four photodiodes, an electronic IC control circuit and the 4x4 DLSPP-based switching matrix. Four 7-wavelength data channels are entering each SOI MUX

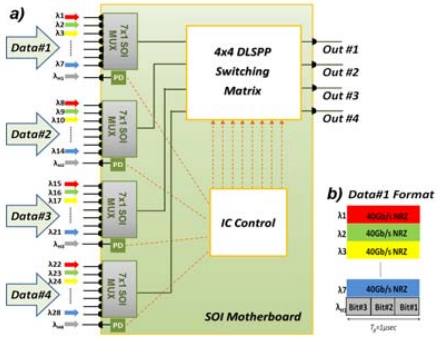

Fig.1. a) The architecture of PLATON's 4x4 Tb/s routing fabric and b) the multiwavelength data packet format.

module and the output of every SOI MUX enters the DLSPP-based switching matrix that is responsible for routing the data streams to the desired outputs. Control of the thermo-optic DLSPP-based switching matrix and switch state determination are obtained by means of the electronic IC circuit after processing the header information of the incoming data streams. Optoelectronic conversion of the four headers is performed in the respective photodiodes residing at the front-end of the SOI motherboard. This platform allows for a total router throughput of 1.12 Tb/s when combined with the multiwavelength data traffic format shown in Fig. 1(b): Each data stream comprises seven time-synchronized, 40Gb/s data carrying wavelengths spaced by 100GHz and being multiplexed into a 280Gb/s common stream via the SOI MUX modules, whereas the low-rate address information for each traffic sequence is carried by a separate wavelength that is inserted directly into the photodiode.

Fig. 2 depicts the basic configuration utilized for enabling the monolithic integration of silicon with plasmonic waveguides. It shows a 340nm high silicon wire interfaced with a 500x600nm^2 DLSPP waveguide that resides on top of a 60nm-thick gold film. Numerical results obtained through the vectorial 3D finite element

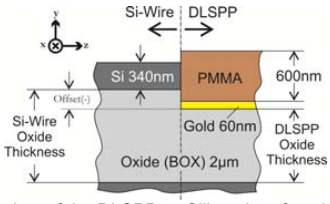

Fig.2. Side-view of the DLSPP-to-Silicon interface layout.

method (FEM), reveal that silicon-DLSPP coupling with ~1dB insertion losses can be achieved for a silicon wire width of 175nm and a vertical offset of 200nm.

Fig. 3(a) and (b) show the layouts of a 4:1 SOI MUX circuit and a 2x2 PMMA-loaded SPP-based dual-ring resonator switch. The SOI MUX comprises four cascaded 2nd order SOI ring resonators and is capable of multiplexing four 40Gb/s wavelengths spaced at 100GHz. This can be confirmed by the MUX transfer function shown in Fig. 3(c) and consisting of 4 resonant peaks, each one having a 0.32nm 3-dB bandwidth. The transfer function of the 2x2 PMMA-loaded SPP switch obtained via FEM is illustrated in Fig. 3(d), both for the unheated (20°C) and heated (120°C) states, clearly showing ring-resonator drop and through port responses with 3-dB bandwidths of 10nm for the drop and 5nm for the through port, respectively. All rings in the SOI MUX design have the same 12.7μm radius with every 2nd order ring configuration having a refractive index variation of Δn= 0.0018 with respect to the refractive index of the previous 2nd order ring stage. This Δn value can be easily achieved via electrical phase tuning elements. The coupling coefficients CRa, CRb and CRc that have been used were equal to 0.18, 0.008 and 0.18, respectively. For the 2x2 switch, the ring radius was 5.25μm and the gaps between ring and straight waveguides were 0.3μm and 0.5μm, respectively.

320 Gb/s 2x2 Router Simulation Results

Fig. 4 shows the layout of the 2x2 silicon-plasmonic router. Eight 100GHz-spaced 40Gb/s NRZ wavelength channels grouped in two 4-wavelength clusters are launched into two 4:1 SOI MUX modules, yielding two data streams at the respective SOI MUX outputs with each stream carrying 160Gb/s of aggregate traffic.

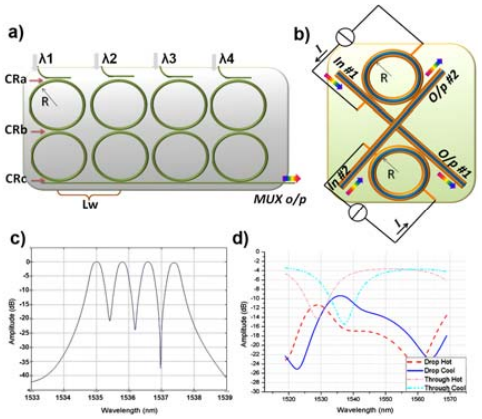

Fig.3. a) 4:1 SOI MUX design, b) 2x2 PMMA-loaded SPP switch, c) 4:1 SOI MUX transfer function, and d) SPP switch transfer function.

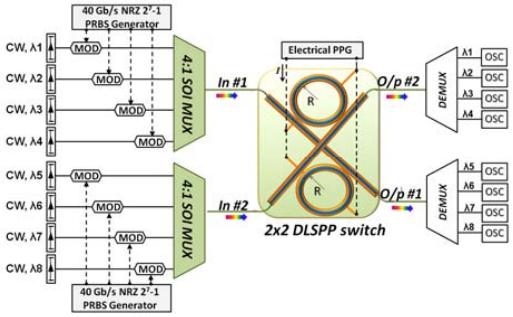

Fig.4. Layout of the 2x2 silicon-plasmonic 320Gb/s router.

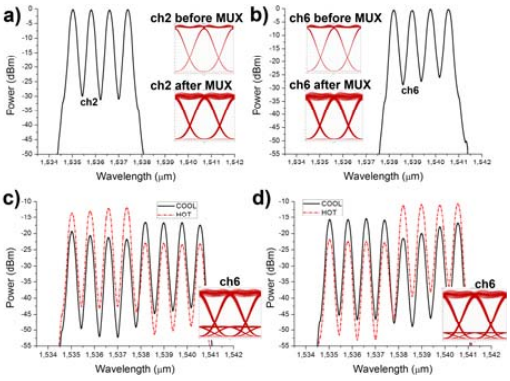

Fig.5. a) and b) Outputs of the two SOI MUX devices, c) and d) multiwavelength signal obtained at the switch outputs #1 and #2, respectively, both for the case of unheated and heated states. Insets in a), b) show the eye diagrams of ch2 and ch6 before and after the SOI MUX, respectively, and insets in c) and d) show the eye diagram of ch6 at the respective switch outputs.

These two optical beams enter a 2x2 PMMA-loaded SPP switch identical to the one depicted in Fig. 3(b).

Fig. 5 shows simulation results obtained by using the VPI physical layer simulation package for the evaluation of the 2x2 router platform. Fig. 5(a) and (b) depict the output signals of the two SOI MUX circuits. Fig. 5(c) illustrates the spectrum of the signal emerging at output#1 of the switch both when operating in its OFF and its ON state, which correspond to unheated (20°C) and heated rings (120°C). The corresponding switch output#2 signal spectra are shown in Fig. 5(d). The insets in Fig. 5(c) and 5(d) depict the eye diagram of the individual channel 6 obtained at the corresponding switch output ports. Successful switching for both 4-wavelength data streams can be confirmed, with extinction ratio values ranging from 6 to 10dB for all eight channels.

Acknowldegment

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