Fabrication and Experimental Demonstration of a Four-Channel × 40 Gb/s TriPleX All-Optical Wavelength Conversion Platform

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***Abstract*—We present a scalable circuit that performs multichannel, all-optical wavelength conversion employing semiconductor optical amplifiers (SOAs) and a densely integrated TriPleX photonic chip. The TriPleX device performs chirp filtering and signal polarity inversion with on-chip signal processing. The chip includes a total number of 40 arrays of Si_3N_4–SiO_2 microring resonators, delay interferometers and heating elements. The total footprint of each array is 2.19 mm^2 and the power consumption per integrated heater is below 80 mW. We have interconnected the TriPleX chip with SOAs and we demonstrate experimentally 4 × 40 Gb/s, parallel and wavelength tunable wavelength conversion with power penalties of less than 3 dB.**

***Index Terms*—Microring resonators, optical signal processing, photonic integration, semiconductor optical amplifiers (SOAs), wavelength converters (WCs).**

I. Introduction

WAVELENGTH DATA ROUTING using compact, low-cost, and power-efficient integrated photonics is considered a promising solution for future ultrafast, high-capacity core networks. In this context, academic and industrial R&D groups have focused their efforts on the development of highly integrated photonic components that perform routing functionalities [1]–[3], buffering [4], wavelength conversion [5]–[7] switching [8], [9], and contention resolution [10]–[12] in the optical domain. The development of ultrahigh capacity routing platforms based on these components requires photonic integration technologies that can provide dense parallel integration to support wavelength division multiplexing (WDM). In addition to large integration density, these components should feature low loss and low power consumption and should be realized with cost-effective fabrication techniques.

One of the key components in photonic routing architectures is the optical wavelength converter (WC). The realization of truly compact and energy efficient terabits per second switching fabrics using scalable all-optical wavelength converters (AOWCs) remains in the top priority of research on broadband photonic routing systems. As such, research activities have been focused on the development of chip-scale, arrayed, WDM WCs using either hybrid or monolithic photonic integration. In this context, the European project IST-MUFINS has demonstrated a quadruple array of 40 Gb/s AOWCs on a chip size of 15 mm × 58 mm, employing silica-on-silicon technology [13]. Recently, other researchers have presented monolithic tunable optical router, a 61.6 mm^2 monolithic InP chip that hosts eight parallel AOWCs [14]. Both approaches have implemented the AOWCs with semiconductor optical amplifier (SOA) Mach–Zehnder interferometers that employ two active elements (SOAs) per AOWC. Simpler AOWCs with reduced feature size can be achieved with chirp-filtering technique that can operate at ultrahigh bit rates (>100 Gb/s) employing only a single active component (a nonlinear SOA) followed by an optical bandpass filter (OBF) [15]. The scheme has originally been demonstrated with bulk OBFs; however, the appearance of microring resonators (MRRs) has enabled the implementation of microring-assisted AOWCs that can guarantee compactness and graceful scaling to WDM architectures. MRR-assisted AOWCs based on silicon-on-insulator can accommodate high-speed data rates due to the high index contrast, the potential for ultrasmall bends and the corresponding short round-trip times that are comparable to the ultrashort pulsewidths used at >100 Gb/s bit rates [17]. However, for bit rates up to 40 Gb/s where the pulses are in the order of tens of picoseconds, medium-index contrast material such as TriPleX is most suitable due to lower waveguide and fiber-coupling loss [18].

Recently, the first report of this scheme employed a single ring resonator and a bulk delay interferometer (DI), comprising

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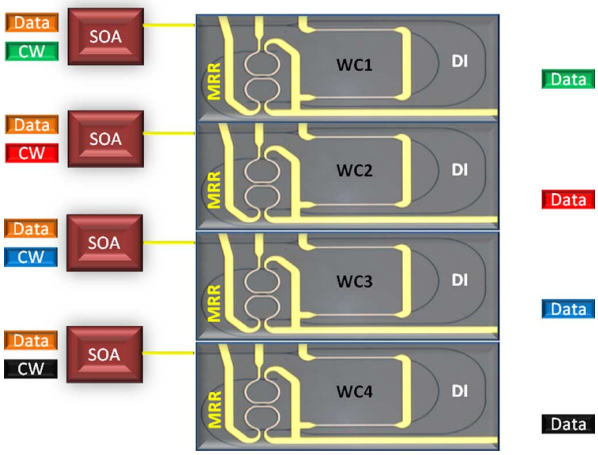

Fig. 1. Concept of the 4 × 40 Gb/s AOWC.

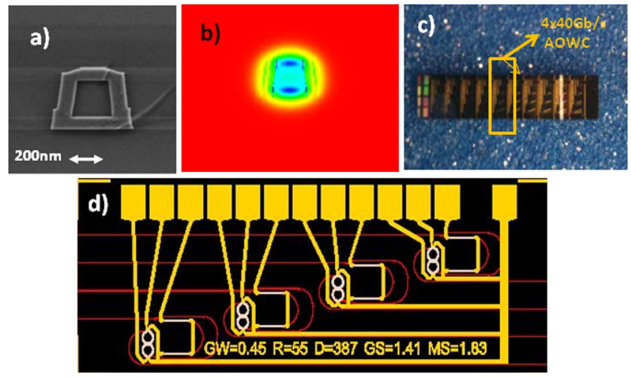

Fig. 2. (a) Box-shaped TriPleX waveguide. (b) Mode Profile. (c) Fabricated device. (d) Mask of the TriPleX chip.

polarization controllers, beam splitters, and polarization-maintaining (PM) fiber [16]. In this single-channel 40 Gb/s proof-of-principle experiment, two erbium-doped fiber amplifiers (EDFAs) were employed within the WC due to the use of discrete components; one EDFA to compensate fiber-to-chip and chip-to-fiber coupling losses of the discrete reconfigurable optical add-drop multiplexer and one for postamplification and compensation of the losses of the cascaded bulk DI. The use of the two EDFAs per WC dominated the overall size and power consumption of the scheme limiting the scalability of a WDM demonstrator. In addition, the power consumption of each integrated heater element was ∼480 mW, raising thermal management and thermal crosstalk issues in the case of dense integration of MRR arrays. In order to develop a compact and low-loss multichannel routing system based on the medium-index contrast TriPleX platform, it was necessary to integrate both the MRR and DI components on the same photonic chip. In addition, further reduction of the power consumed by the heater elements would be required to relax thermal management issues and enable a more dense integration level.

In this paper, we demonstrate the first multichannel wavelength conversion TriPleX platform that integrates arrays of second-order MRRs and DIs on the same photonic chip. Due to the on-chip interconnection of the MRRs with the DIs, no in-line optical amplification is required restricting the total size of the scheme to 87.5 mm^2. Both MRRs and DIs can be independently tuned by heater elements each one consuming only 80 mW of electrical power. We demonstrate error-free, 4 × 40 Gb/s wavelength tunable, all-optical wavelength conversion with <3 dB power penalty.

II. Principle of Operation

Fig. 1 shows the 4 × 40 Gb/s AOWC scheme. In this concept, four external SOAs are interconnected with a TriPleX integrated circuit that features four independent line structures. Each of them comprises a second-order ring resonator followed by a DI. Data streams enter the SOAs together with continuous wave (CW) light to which wavelength conversion has to be performed. Due to the finite recovery time of the SOAs, the wavelength converted signals suffer from distortion. SOA speed up is accomplished by using the TriPleX chip. First, the signals pass through a second-order MRR that performs chirp-filtering and effective recovery suppression. This can be achieved by detuning the response of each MRR slightly off the CW wavelength peaks using the integrated heating elements. In the case of blue-shifted offset filtering, inverted signals are generated at the output of the MRRs and the signal polarity needs to be restored. For this reason, all the drop ports of the MRRs are waveguide interconnected to arrays of tunable DIs whose notches are used for CW carrier suppression and to obtain noninverted operation. Finally, the data streams exit the AOWC platform imprinted on the CW wavelengths. The integration of the MRRs and DIs on the same chip implies that no in-line amplification is required, enabling the scaling of this scheme in terms of throughput, power consumption, and footprint.

III. Device Fabrication

The key components for the 4 × 40 Gb/s AOWC is the arrayed structure of MRRs and DIs. The whole integrated circuit was fabricated using TriPleX waveguide technology developed by LioniX, Enschede, The Netherlands. Stoichiometric silicon nitride (Si_3N_4) fabrication using low-pressure chemical vapor deposition (LPCVD) processing is widely used in integrated optics because of its large refractive index ($n \sim 2.0$) that enables very compact devices. By combining an additional material having a large compressive stress, such as LPCVD silicon dioxide (SiO_2), the total stress of the composite layer stack is strongly reduced. This alternating LPCVD layer stack concept can result in a rectangular channel waveguide structure with outstanding waveguiding characteristics and strong polarizing effects. This waveguide structure is formed by a cross section of silicon nitride (Si_3N_4) filled with and encapsulated by SiO_2, as shown in Fig. 2(a). The channel geometry approximates a "hollow core" system, since it consists of a low-index "inner core" of SiO_2 "cladded" with the high-index "outer core" of Si_3N_4. Modal characteristics depend only upon the geometry of the structure, as all composing materials are LPCVD end products with very reproducible characteristics. The whole process is CMOS compatible and very cost effective since only one photolithographical step is required for waveguide definition and guarantees a propagation loss of <0.1 dB/cm [18].

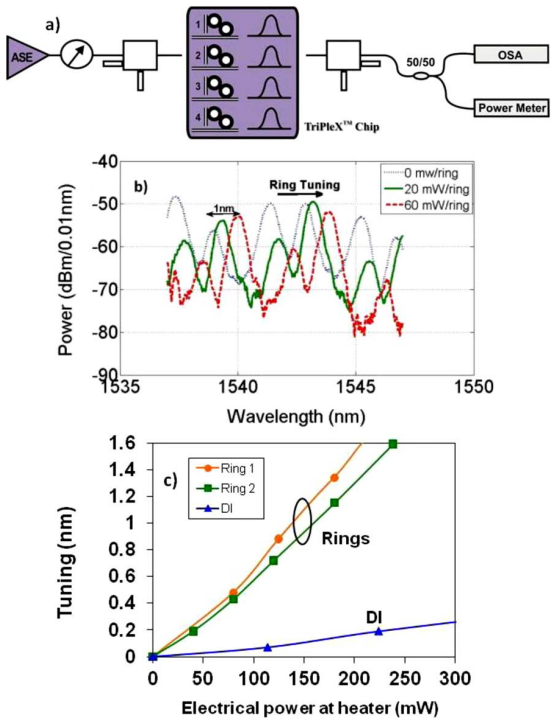

Fig. 3. (a) Characterization setup. (b) MRR wavelength tuning. (c) Tuning versus power.

The fabrication process starts with thermal oxidation of a 100 mm diameter silicon wafer to form the lower cladding. Then, Si_3N_4 and SiO_2 are deposited by LPCVD and the photolithographical step is performed together with reactive ion etching. After a second LPCVD deposition of Si_3N_4, local removal of the slab nitride layer is performed, followed by the top-cladding deposition. Local removal of the nitride, although more difficult in fabrication, results in a box-shaped structure reducing the modal birefringence and, also important, the absence of slab waveguides. The last two steps are LPCVD and plasma-enhanced chemical vapor deposition based oxide depositions to form the upper cladding. After the top-cladding depositions, the top surface is planarized by chemical mechanical polishing to yield a flat surface. A thin film of chromium and gold is deposited by electron-beam evaporation. These films are subsequently patterned with a two-step lithographical process using standard contact lithography and wet chemical etching to fabricate the microheater structures. The gold is etched near the ring resonators to locally increase the resistance. The silicon of the waveguide at the position of the heater was underetched reducing the leakage of heat to the silicon substrate. Although tuning speed was limited, tuning power was decreased to $\sim$80 mW due to the concentration of the heat in the waveguide. The box-shaped waveguide had a 450×450 nm SiO_2 core with a 170 nm Si_3N_4 shell, allowing MRR bend radii down to 55 μm. Fig. 2(c) illustrates the final TriPleX chip and the section that was chosen for the 4×40 Gb/s AOWC experiment. Fig. 2(d) shows part of the mask design with a set of pads for MRR and DI wavelength tuning.

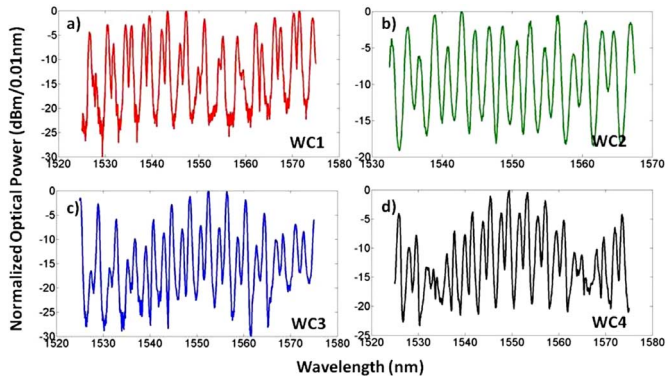

Fig. 4. Transfer functions of WC1–WC4. The power has been normalized to the transmission peak in the spectrum.

TABLE I
OPTIMUM OPTICAL AND ELECTRICAL POWER LEVELS FOR WCS

WC / Power	*WC1* *1559nm*	*WC2* *1561nm*	*WC3* *1557nm*	*WC4* *1550nm*
opt. PData	1.6 mW	3.13 mW	2.92 mW	2.53 mW
opt. PCW	0.747 mW	0.627 mW	0.57 mW	0.8 mW
el. PHeater (1st ring)	131.44 mW	0.88 mW	0 mW	0 mW
el. PHeater (2nd ring)	0 mW	0.88 mW	0 mW	0 mW
el. PHeater (DI)	0 mW	85.68 mW	0 mW	69.7 mW

IV. Device Characterization

Fig. 3(a) depicts the experimental setup for the characterization of the TriPleX chip. Amplified spontaneous emission from a spectrally flat light source was used for capturing the MRR and DI responses. A single polarization state was achieved utilizing a polarizer with over than 30 dB polarization extinction ratio. The light was coupled into the chip through a PM-lensed fiber, and the spectral response was acquired by an optical spectrum analyzer with a resolution of 10 pm. Fig. 3(b) shows the tuning of the MRR response when both ring heaters are enabled. With 60 mW/ring, wavelength tuning of 1 nm was achieved. Fig. 3(c) illustrates the individual heater tuning with respect to the electrical power.

Fig. 4 depicts the transfer functions of all the AOWCs. The free spectral range (FSR) of MRRs and DIs was 4 nm, while the 3 dB bandwidth was 60 GHz. An extinction ratio of $>$18 dB was achieved when MRRs and DIs were tuned properly. Due to fabrication tolerances, there was a slight difference between the FSRs of MRRs and DIs. This resulted in a nonuniform spectral response, which could be optimized with the heating elements at the operating wavelength inside the full *C*-band.

V. Experiment

The 40 Gb/s data signal was generated by time interleaving the pulses from a 2.2 ps, 10 GHz, tunable, mode-locked laser modulated with a $2^7 - 1$ pseudorandom bit sequence and tuned to a different transmission peak for each of the MRR/DI sequences (see Fig. 5). A pigtailed commercially available SOA with a gain recovery time of 30 ps was used for cross-gain

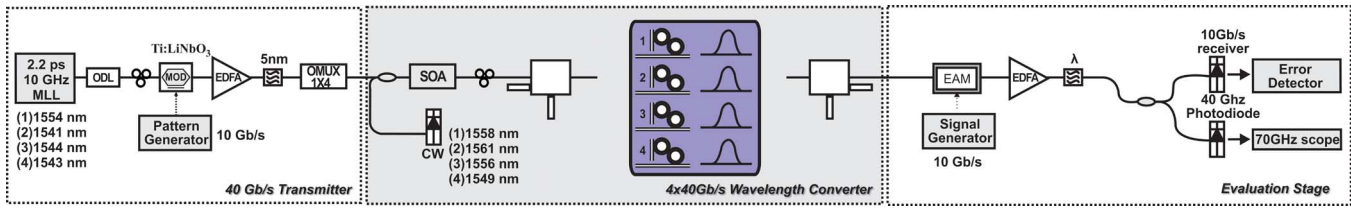

Fig. 5. Experimental setup.

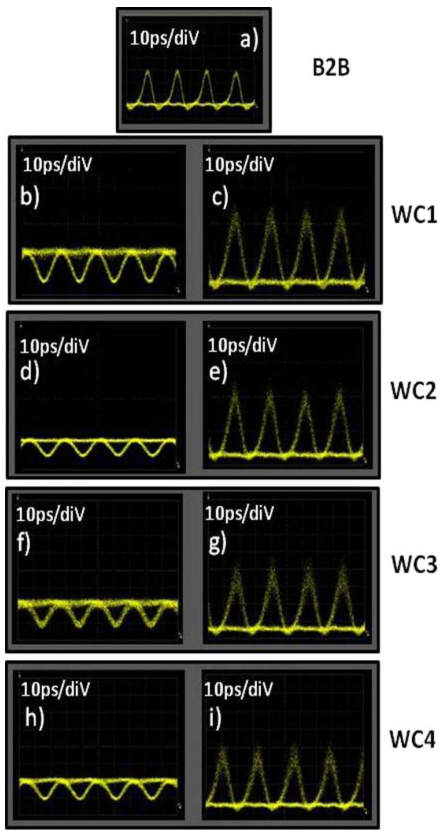

Fig. 6. Eye diagrams of (a) B2B signal, (b), (d), (f), (h) inverted signals at the output of WC1–WC4, and (c), (e), (g), (i) noninverted signals at the outputs of WC1–WC4, respectively.

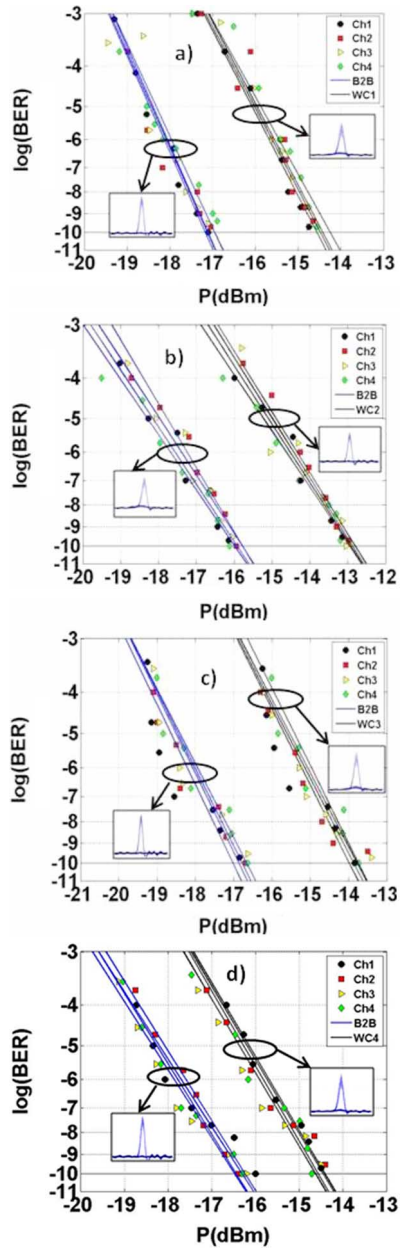

Fig. 7. BER curves of (a) B2B and WC1, (b) B2B and WC2, (c) B2B and WC3, and (d) B2B and WC4.

and -phase modulation, and four laser diodes for providing the CW signals. The chip coupling was performed through standard single-mode lensed fibers. The outputs of the four WC signals at 40 Gb/s were evaluated by bit-error-rate (BER) measurements after demultiplexing to 10 Gb/s using an electroabsorption modulator. Table I shows the optimum operating power levels used for each WC. Deviations in the optical power measurements are primarily due to the SOA spectral profile and different fiber-to-waveguide coupling losses. The average electrical power required to tune the filter elements of each WC was 72 mW, or 24 mW per heater.

The eye diagram of the incoming data stream is depicted in Fig. 6(a). By detuning the transmission peaks of the second-order ring resonators 0.2 nm (blue-shifted) off the CW carriers, inverted operation is achieved at the outputs of the four WCs as illustrated in Fig. 6(b), (d), (f), and (h). With further tuning (0.3 nm blue-shifted), the inverted signal peaks approach close to the notches of the DIs and as a consequence the signal polarity is restored. Fig. 6(c), (e), (g), and (i) shows these noninverted signals, verifying the SOA recovery acceleration and the effective increase of system operational speed. Initial and converted wavelengths for the four parallel WCs were 1) 1554 to 1558

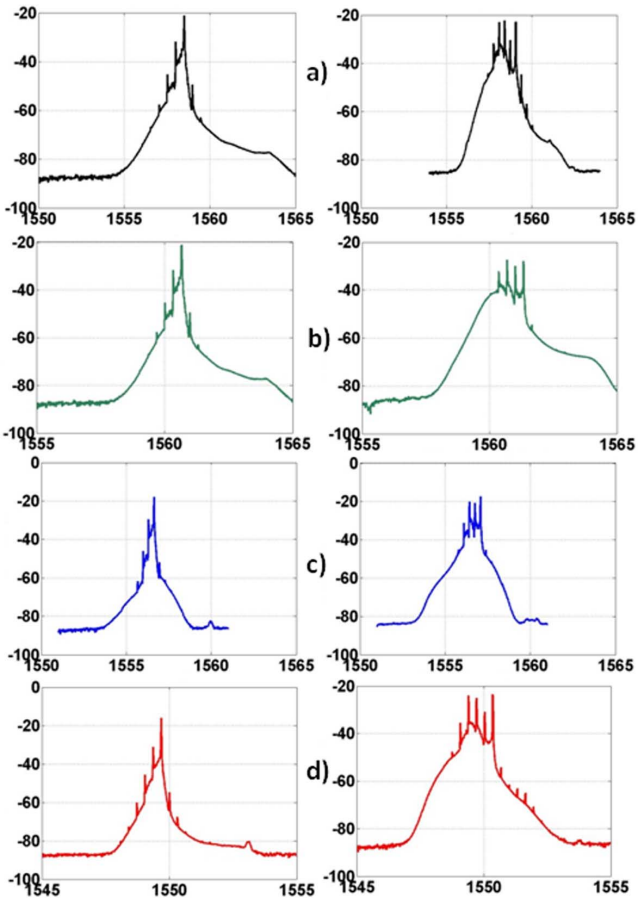

Fig. 8. Inverted and noninverted spectrums for (a) WC1, (b) WC2, (c) WC3, and (d) WC4 [P(dB·m)-λ(nm)].

nm, 2) 1541 to 1561 nm, 3) 1544 to 1556 nm, and 4) 1543 to 1549 nm.

Fig. 7 depicts the BER curves obtained for the back-to-back and WC signals. Error-free operation was measured for all the demultiplexed, wavelength converted signals, with power penalties of less than 3 dB. No signal amplification was required between the SOA and the TriPleX chip, and the power penalty could be further reduced with fiber-to-chip coupling with tapered waveguide facets. Fig. 8 shows the optical spectrums recorded for all the four individual WCs. In the left-hand side, the inverted wavelength converted spectrums are depicted where slight blue-chirp filtering has been performed. On the right-hand side, noninverted spectrums are represented where carriers have been sufficiently suppressed by the DI notches.

VI. Conclusion

We have demonstrated the fabrication and testing of the first TriPleX wavelength conversion platform that offers 4×40 Gb/s throughput on a total footprint of 8.75 mm^2. The TriPleX chip consumes <80 mW of electrical power per heater element to tune each of the 12 optical components. By tuning the arrays of second-order MRRs and DIs, we have presented 40 Gb/s all-optical wavelength conversion with power penalties of less than 3 dB.

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