Experimental Demonstration of an All-Optical Packet Forwarding Gate Based on a Single SOA-MZI at 40 Gb/s

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Abstract: We present a new forwarding-gate scheme using a single SOA-MZI. We show a bi-stable behavior with a 13.6 dB extinction-ratio and rise and fall times below 30ps. Error-free operation is achieved at 40 Gb/s.

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1. Introduction

Photonic switching subsystems have been established as key elements of future optical networks providing ultra-fast signal processing functions and the capability to operate with hundreds of Gb/s data rate [1]. In addition, recent developments in photonic integration technology have shown that the fabrication of small footprint intelligent all-optical photonic structures is now feasible, thus paving the way to the deployment of such circuits in near future networks [2]. However, there are still obstacles to be overcame regarding the implementation of these circuits, most notably the design of core all-optical modules such as optical flip-flops and packet switching elements, which are vital for the development of more complex structures.

Most of the optical flip-flop and packet switching schemes that have been presented so far are based on SOA-MZIs [3,4]. The major benefits of these modules are their stable operation and integrability into compact, switching units. Successful demonstrations of SOA-MZI flip-flop circuits include, among others, integrated solutions with coupled SOA-MZIs [3] and single SOA-MZI based implementations with a feedback loop [4]. Furthermore, a forwarding operation function was also achieved using a flip-flop cascaded with an AND gate [5]. Even though these solutions trail blazed implementations of flip-flop circuits and forwarding gates underlining their potential, they present disadvantages such as low switching responses and the use of more than one optical structures.

In this paper we demonstrate a new all-optical packet-forwarding gate based on a single SOA-MZI. The scheme takes advantage of the stable and ultrafast capabilities of the flip-flop configuration that has been presented and analyzed theoretically in [6] in order to forward data through the same module. The proposed scheme provides an extinction ration of about 15 dB with a rise and fall time below 30ps. Error-free operation was achieved at 40 Gb/s.

2. Principle of operation

Figure 1 shows the principle of operation of the proposed forwarding gate. A CW signal is inserted to port 5 of the SOA-MZI serving as the output wavelength of the flip-flop. With the absence of control signals, no optical power is obtained at the output of the lower branch of the SOA-MZI (port 8) resulting in the OFF state of the flip-flop (port 7). In order to switch the states of the flip-flop, Set and Reset control pulses are launched into ports 1 and 3 of the SOA-MZI, respectively. With the introduction of a Set pulse at port 3, the carrier density of SOA2 is reduced and thereby its gain. As a result, the two branches of SOA-MZI become unbalanced, performing this way a switch of the signal power at the output port of the flip-flop (ON state). In order to maintain this state, a continuous flow of control power must be passed through SOA2. This task is accomplished by the feedback loop, which forwards a portion of the optical CW output power through the external coupler again to SOA2 when the Set pulse exits the lower branch at port 6. To return to the OFF state, a Reset pulse is introduced into port 1 of the SOA-MZI resulting in the reduction of SOA1's carrier density and gain [6]. The time duration of Set and Reset pulses is equal to the round trip time in the feedback loop so as the CW beam to reach the lower SOA retaining its gain suppression [6].

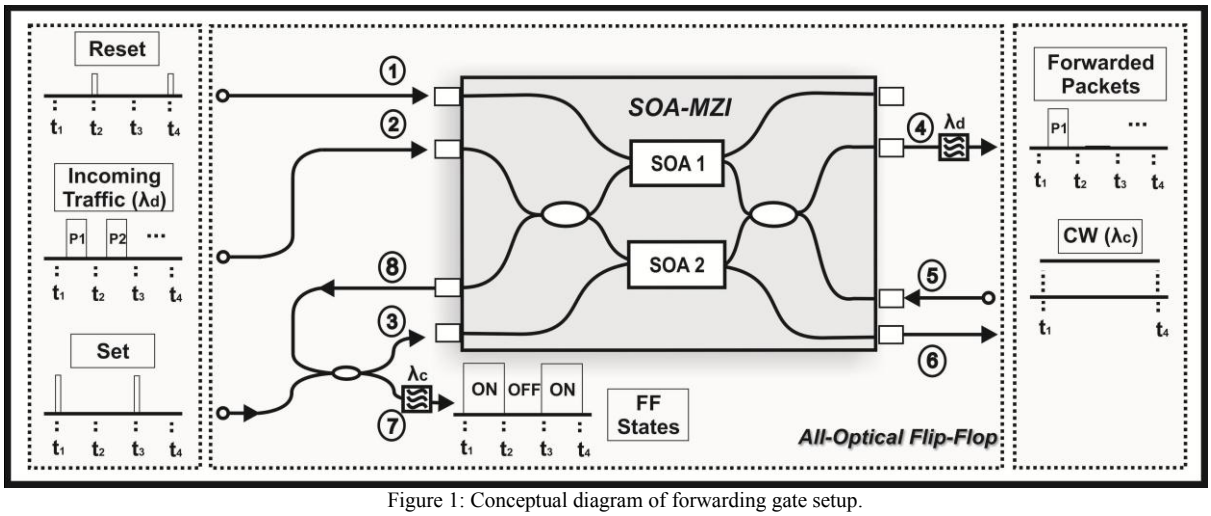

Figure 1: Conceptual diagram of forwarding gate setup.

For the forwarding operation to take place, data packets are inserted into the SOA-MZI from port 2. This data signal is equally split into two parts and then propagates through the two MZI branches respectively, reaching the two SOAs of the module and reducing their carrier densities and gains almost by the same quantity. The data streams, experience the same function as the CW beam and therefore through interference at port 4, the packets come out when the flip-flop is in ON state and blocked otherwise. Accordingly, forwarding operation is achieved when a data packet is fed into the gate along with a Set and a Reset pulse. The Set pulse is synchronized with the leading edge of the incoming data packet while the Reset pulse coincides with the end of the packet. The Set pulse turns the flip-flop ON and allows the packet to propagate to its destination whereas the second pulse will turn it OFF so that further packets will be blocked.

3. Experiment and results

The experimental setup of the proposed all-optical forwarding gate is shown in Figure 2a. A pulse-train of ~3 ps pulses at 1552.31 nm from a 40 GHz mode-locked laser (MLL) was inserted into a Ti:$LiNbO_3$ modulator, driven by a PRBS pattern generator, yielding a 40 Gb/s 2^7-1 RZ data sequence at its output. This signal was then re-modulated by a 10 Gb/s pattern generator in order to form a sequence of two data packets of 152.4 ns duration. Two CW signals at 1558.17 nm and 1559.79 nm were used for the generation of the Set and Reset pulses of the flip-flop, respectively. The two CW signals were initially multiplexed and fed into a Ti:$LiNbO_3$ modulator driven by a 10 Gb/s pattern generator. The output of the modulator was then amplified and inserted into an AWG for the Set and Reset pulse streams to be separated. In order to set the appropriate time interval between the two control signals (Set/Reset), an optical delay of 100m SMF was introduced in the "Reset" path leading to an approximate delay of 500 ns and a repetition period of 990.6 ns. The width of Set and Reset pulses was 32.1 ns, equal to the length of the feedback loop.

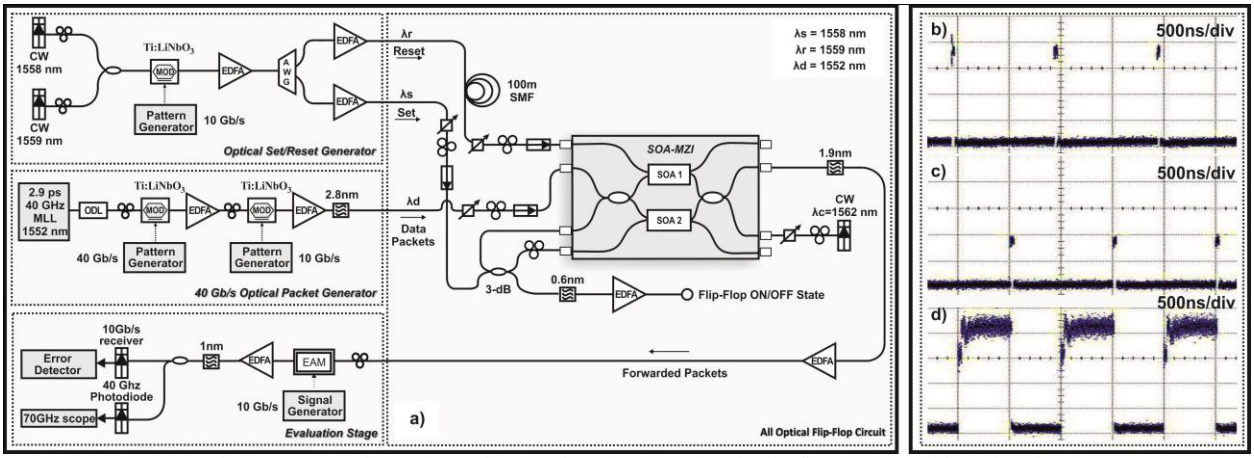

Figure 2: a) Experimental setup b) Set pulses c) Reset pulses d) Flip-flop response with no data signal.

In order to evaluate the performance of the proposed forwarding gate, a CW signal at 1562,23 nm was initially introduced to the SOA-MZI without the use of the data signal. Set and Reset pulses effectively switched the output states of the flip-flop resulting in a contrast ratio of 13.6 dB, with a rise-time of 29 ps and a fall-time of 22 ps as depicted in Figures 2b, 2c and 2d. The power levels of the CW, Set and Reset signals were -2.57, -3.92 and -7.54 dBm, respectively. The two generated data packets were then launched into the flip-flop configuration (Figure 3b) with a power level of -2.7 dBm. The first packet was delimited by Set and Reset pulses and was synchronized, as previous mentioned, with the ON state, whereas the second packet was synchronized with the flip-flop's OFF state. Figure 3e shows the first packet, which is correctly forwarded, while the second one was totally suppressed resulting in an extinction ration of about 15 dB. A clear eye-diagram of the forwarded packet is shown in Figure 3f.

Figure 3a shows BER measurements obtained at the output of the proposed scheme. Each BER curve corresponds to the worst performing between the four 10 Gb/s tributaries, which are associated with the 40 Gb/s signal. Error free operation with power penalty of about 4 dB was achieved for the output packet.

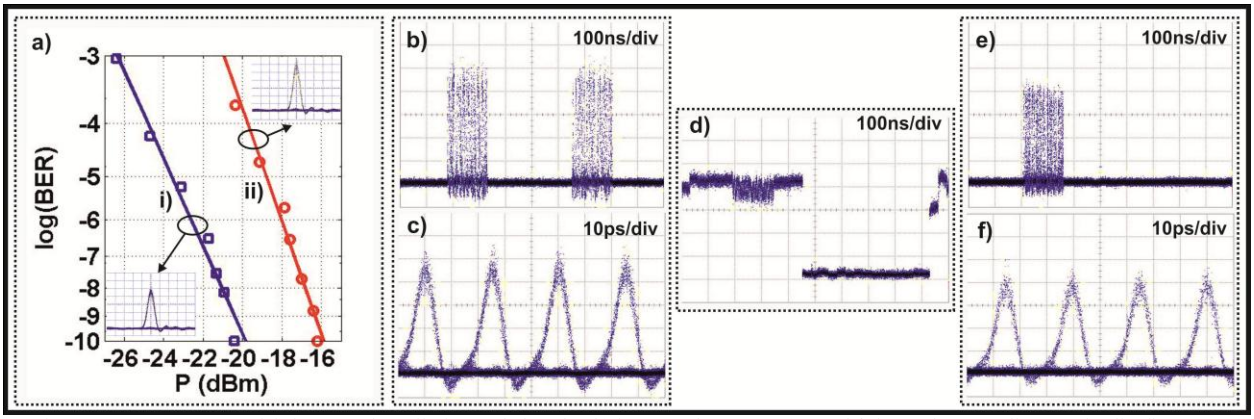

Figure 3: a) BER curves of i) input packets, ii) forwarded packet b) input packets trace c) 40 Gb/s input data eye-diagram d) Flip-flop state (port7) e) forwarded packet trace f) 40 Gb/s forwarded packet eye-diagram.

4. Conclusions

We have experimentally demonstrated a new all-optical forwarding gate based on a flip-flop circuit comprised of a single SOA-MZI with feedback. Error-free functionality was achieved at 40 Gb/s. The performance of the proposed gate can be greatly enhanced by means of optical integration.

Acknowledgment

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