4x40 Gb/s All-Optical Wavelength Conversion Using SOAs and Integrated Arrays of Ring Resonators and DIs

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Abstract: We present 4x40Gb/s all-optical wavelength conversion employing SOAs fiber-interconnected with integrated arrays of tunable Si_3N_4–SiO_2 micro-ring resonators and delay interferometers. We demonstrate chirp filtering and polarity inversion on-chip.
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1. Introduction

Photonic integration of scale is the key to achieve compact, power efficient and scalable super chips that will enable the development of high performance optical routing systems. In this context, integration efforts have focused on the miniaturization and dense integration of arrays of passive photonic elements -including Micro-Ring Resonators (MRRs) and Delay Interferometers (DIs)- that can be applied in WDM networks as wavelength selective switches [1,2] or buffering structures [3]. Recently we have demonstrated a single MRR-assisted all-optical wavelength converter (AOWC) at 40Gb/s in a proof of principle experiment that required optical fibers and amplifiers for component interconnection and loss compensation [4]. In the present communication we extend this work and show a 4x40Gb/s AOWC that employs a SOA and a chip with an integrated array of tunable ring resonators and DIs based on the TriPleX^{TM} fabrication process [5]. The TriPleX^{TM} chip includes four independent line structures, each comprising of a 2nd order ring resonator for chirp-filtering and SOA recovery acceleration, followed by a DI for signal polarity inversion. The total footprint of the chip is 8.75mm^2 and it includes integrated heating elements that are used to spectrally adjust the MRRs and DIs. Besides its small footprint, the new chip allows for the independent tuning of the spectral responses of each element in the integrated array of MMRs and DIs so that WDM-functionalities required in a routing matrix are accommodated on a single chip. Additionally the sequential MRR and DI arrayed integration on a single chip avoids pigtailing and reduces circuit losses so that no amplification is required between the MRR and the DI, resulting in a truly compact circuit.

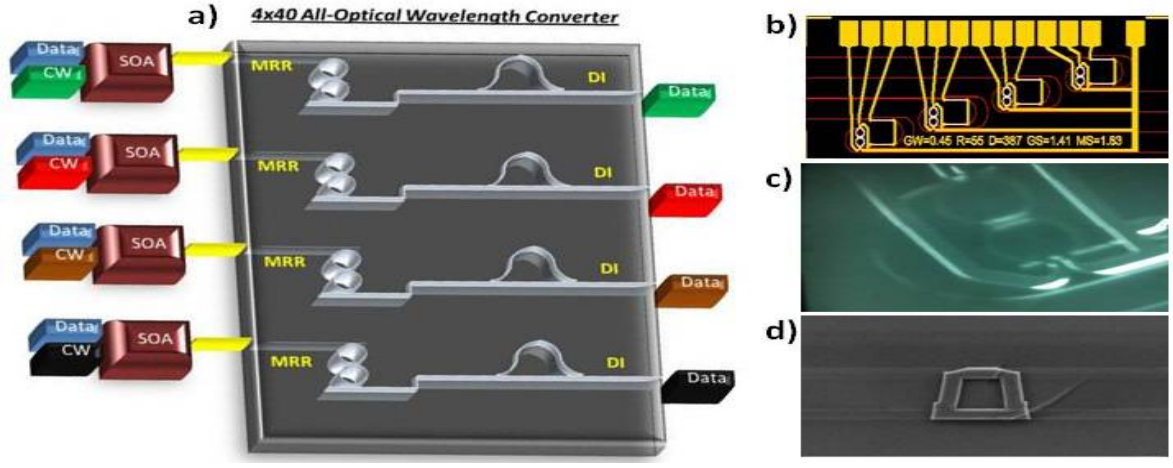

Figure 1: a) Concept of 4x40 AOWC, b) Mask of TriPleX^{TM} chip, c) 2nd Order Ring Resonator View, d) SEM of TriPleX^{TM} Waveguide

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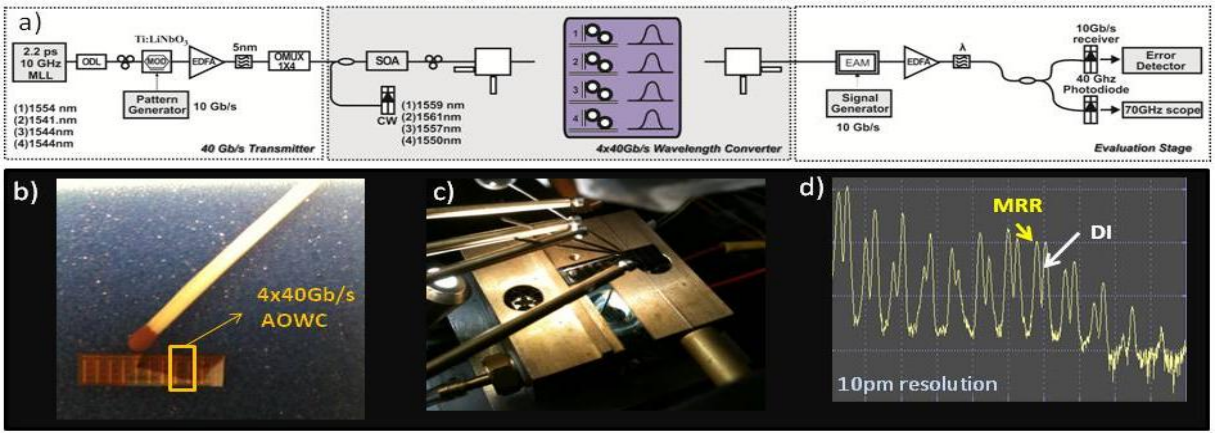

Figure 2: a) Experimental setup, b) TriPleX^{TM} chip, c) Fiber and probe alignment, d) MRR and DI spectral responses in case of ASE seed

2. Concept and Experimental Setup

Figure 1a) depicts the 4x40 Gb/s AOWC concept, featuring 4 external SOAs fiber-interconnected to a TriPleX^{TM} chip with integrated arrays of 2nd order ring resonators and DIs. 40 Gb/s data streams enter each of the SOAs together with CW signals to which the original data streams are to be wavelength converted. Wavelength conversion to different wavelengths is achieved by selection of the CW signal and tuning of the spectral characteristics of the MRRs and DIs. XGM-XPM takes effect resulting in distorted wavelength converted signals due to the saturation and finite recovery of the SOAs. In order to speed up the overall performance, chirp filtering is applied by detuning the transmission peaks of the 2nd order ring resonators with respect to the CW wavelengths. Each 2nd order ring resonator comprises of two coupled Si_3N_4–SiO_2 ring resonators with 55μm radius of curvature, 500 GHz free spectral range (FSR) and 60 GHz 3dB-bandwidth. The spectral response can be independently tuned through a full FSR using heating elements with less than 80mW each. Figure 1b) illustrates the whole mask design with a number of pads for ring and DI wavelength tuning. When blue-shifted offset filtering is employed, inverted signals are produced after the SOAs. Consequently, the signal polarity has to be restored. For this reason the drop ports of the MRRs are waveguide-interconnected with 2 ps tunable DIs for carrier suppression and signal inversion. Figures 1c),d) show a close camera view of a 2nd order ring resonator and a SEM image of a 450nm width TriPleX^{TM} box-shaped waveguide. Figure 2a) shows the experimental setup in which the four MRR/DI sequences were evaluated separately. The 40 Gb/s data signal was generated by time-interleaving the signal from a 2.2 ps, 10 GHz, tunable, mode-locked laser modulated with a 2^7-1 PRBS and tuned to a different transmission peak for each of the MRR/DI sequences. Four DFB lasers were used to provide the CW signals for the WC and a single discrete SOA pigtailed with a lensed fiber was used to couple the cross-gain and phase modulated signals into the input waveguide of each filter sequence under test of the TriPleX^{TM} chip for chirp filtering and polarity inversion. Figure 2b) shows the chip and the section that was used for 4x40Gb/s WC. Figure 2c) depicts a view of the TriPleX^{TM} chip on the vacuum chuck, the tips and the input/output lensed fibers, while figure 2d) illustrates the spectral responses of both, the 2nd order ring resonator and the DI. The outputs of the four output WC signals at 40Gb/s were evaluated by BER measurements after demultiplexing to 10 Gb/s using an Electro-Absorption Modulator (EAM). Table I shows the optimum optical power levels used into the SOA for the 4 separate WCs.

	WC1@1559nm	WC2@1561nm	WC3@1557nm	WC4@1550nm
P_{Data}	1.6 mW	3.13 mW	2.92 mW	2.53 mW
P_{CW}	0.747 mW	0.627 mW	0.57 mW	0.8 mW

Table I: Optimum powers levels for WCs

3. Results and Discussion

The eye-diagram of the incoming data stream is depicted in figure 3a). Figure 3b) shows the signal directly at the output of the SOA, indicating its slow recovery time. By detuning the transmission peaks of the 2nd order ring resonators 0.2nm (blue-shifted) off the CW carriers, inverted operation is achieved at the outputs of the 4 WCs as illustrated in figures 3c),d),g),h). With further tuning (0.3nm blue-shifted) the inverted signal peaks approach close to the notches of the DIs and as a consequence the signal polarity is restored. Figures 3e),f),i),j) show these non-inverted signals, verifying the SOA recovery acceleration and the effective increase of system operational speed.

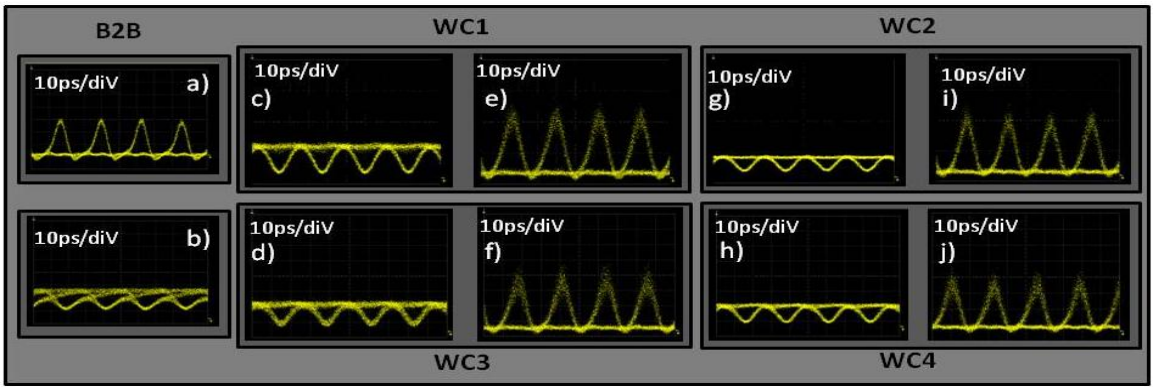

Figure 3: Eye-diagrams of a) B2B signal, b) SOA recovery, c),g),d),h) Inverted signals at the output of WC1, WC2, WC3,WC4, e),i),f),j) Non-Inverted signals at the outputs of WC1, WC2, WC3,WC4 respectively.

Figure 4 depicts the BER curves obtained for the back-to-back and WC signals. Error-free operation was measured for all the demultiplexed, wavelength converted signals, with power penalties of less than 3dB. No signal amplification was included between the SOA and the TriPleX^{TM} chip and this power penalty can be further reduced if coupling losses in and out of the TriPleX^{TM} chip are minimized with tapered waveguide facets.

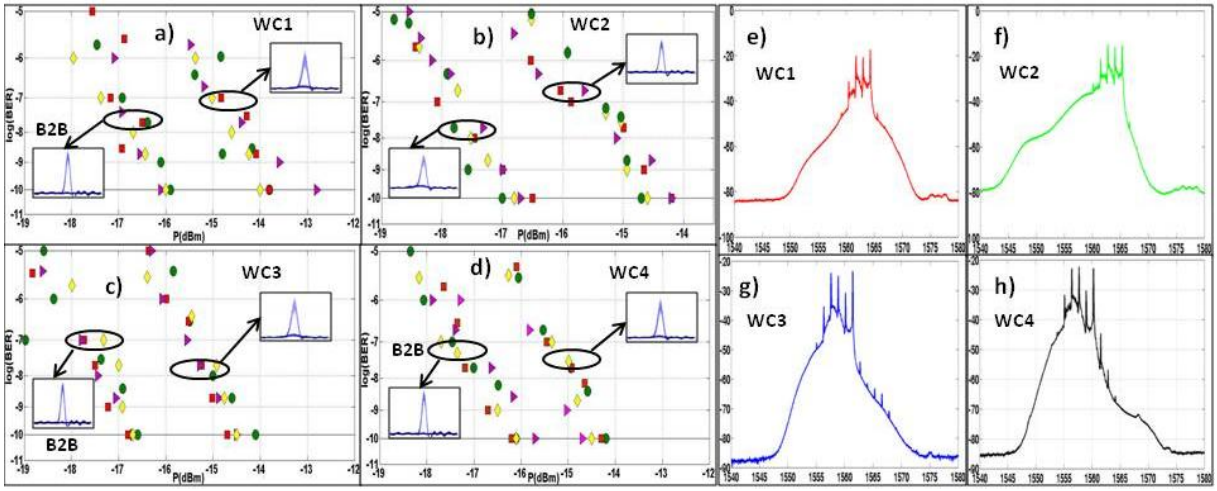

Figure 4: BER curves of a) B2B and WC1, b) B2B and WC2, c) B2B and WC3, d) B2B and WC4, e-h) Non-Inv. Spectra

4. Conclusions

We have performed four-channel 40Gb/s wavelength conversion on a TriPleX^{TM} chip that has a total footprint of 8.75mm^2. By tuning the arrays of 2nd order ring resonators and DIs with heating elements, we recorded inverted and non-inverted operation on-chip with power penalties less than 3dB.

5. References

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