Data Transmission and Thermo-Optic Tuning Performance of Dielectric-Loaded Plasmonic Structures Hetero-Integrated on a Silicon Chip

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***Abstract*— We demonstrate experimental evidence of the data capture and the low-energy thermo-optic tuning credentials of dielectric-loaded plasmonic structures integrated on a silicon chip. We show 7-nm thermo-optical tuning of a plasmonic racetrack-resonator with less than 3.3 mW required electrical power and verify error-free 10-Gb/s transmission through a 60-μm-long dielectric-loaded plasmonic waveguide.**

***Index Terms*— Data transmission, dielectric-loaded surface plasmon polariton waveguides, plasmonics, silicon photonics, thermo-optic switching.**

I. Introduction

ENTERING the area of exascale computing, the roadmap for a future-proof interconnect technology is clearly shaped within the framework of high bandwidth, small footprint and low energy on-chip deployments [1]. In view of this emerging necessity, the exploitation of plasmonics has recently attracted the attention of the photonics community for next-generation chip-scale interconnect purposes, aiming to profit from their small-footprint and low-energy characteristics [2]. The main promise for low power operation comes from the Dielectric-Loaded Surface Plasmon Polariton (DLSPP) waveguide platform, where the metallic layer is additionally equipped with a polymer load on top. The DLSPP platform allows for an enriched functional portfolio through the utilization of the polymer loading properties, while the employment of the metallic film for guiding both light and electrical current raises significant promise for reduced energy consumption requirements [2]–[6].

These unique benefits come, however, at the cost of increased propagation losses that are associated with field penetration in the metal regions, severely restricting the system-level practical application potential of DLSPP structures. A significant number of efforts towards counteracting this drawback has focused on interfacing the DLSPP waveguide platform with the low-loss silicon photonic waveguide technology [7], proposing the use of silicon waveguides for on-chip transmission and passive circuitry functions and the employment of DLSPP components only where low-energy active processes are required [4]. However, the data transfer characteristics of DLSPPs remain still to be addressed before proceeding to functional DLSPP circuitry deployments. At the same time, their low-power credentials have yet to be experimentally confirmed, since the limited number of thermo-optic tunable DLSPP resonator structures demonstrated so far require power levels well beyond a few hundreds of mWs [5]–[6].

In this letter, we present for the first time to our knowledge a solid experimental proof of the data capture and low-energy properties of DLSPP structures integrated on a Silicon-on-Insulator (SOI) waveguide platform. We demonstrate thermo-optic tuning of a Polymethylmethacrylate (PMMA)-loaded SPP racetrack ring resonator over a 7nm wavelength range requiring only 3.3mW of electrical power. Moreover, we report on the first data transfer experiments in DLSPP waveguides with the error-free transmission of a 10Gb/s Non–Return–to–Zero (NRZ) signal through a 60μm long DLSPP waveguide, revealing a power penalty of <0.2dB. Our results confirm the potential of the DLSPP-on-SOI platform to elevate plasmonic technology to energy-effective system-level applications with true data traffic conditions.

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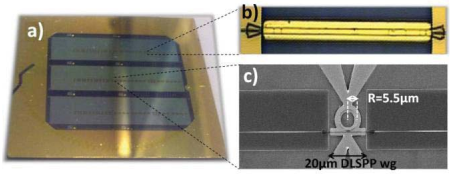

Fig. 1. (a) Real view of Si-Plasmonic chip. (b) Microscope image of the 60-μm-long DLSPP waveguide. (c) SEM image of an ll-pass racetrack ring resonator.

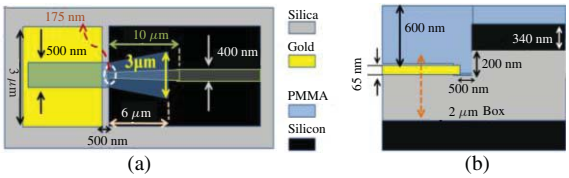

Fig. 2. Schematic of DLSPP to Si-rib waveguide transition: (a) top and (b) side view.

II. Si-To-DLSPP Coupling and Chip Characterization

Figure 1(a) illustrates the Silicon-Plasmonic chip comprising three Silicon-on-Insulator motherboards, properly configured to enable the hybrid integration of plasmonics. The hosting areas of the plasmonic structures on each motherboard have been etched forming 200nm-deep cavities in the Silicon Dioxide substrate. The cavities were covered with 65nm-thick and 3μm wide gold film, on top of which a strip of Polymethylmethacrylate (PMMA) dielectric material with a cross-section of 500 $\times$ 600 nm^2 was placed, forming DLSPP waveguide configuration on silicon dioxide substrate. Figure 1(b) shows a 60μm long straight DLSPP waveguide that has been used for the data transmission experiment and Figure 1(c) depicts a thermo-optic tunable plasmonic racetrack ring resonator with 5.5μm radius of curvature, 0.35μm gap and 0.8μm interaction length, followed by 20μm straight DLSPP waveguides. As DLSPP waveguides support only Transverse Magnetic (TM) field propagation, the SOI motherboard was equipped with TM grating couplers and employed 400 $\times$ 340 nm^2 silicon rib waveguides with 50nm-thick slab in order to allow low-loss TM light propagation. The propagation losses of silicon rib waveguides were measured at 4.42 dB/cm and the per-facet TM grating coupling losses were found to be 12.58 dB.

The interfacing of the Silicon to the DLSPP waveguides was realized by means of a butt-coupling approach relying on the design proposed in [4]. Figure 2 provides a top- and a side-view of the Si-to-DLSPP coupling interface. The silicon waveguides are tapered down from their nominal 400nm width to a width of 175nm prior facing the DLSPP waveguide section. A longitudinal gap of 0.5μm has been used between the silicon waveguide and the metallic stripe in order to avoid possible Si-gold overlapping due to the 0.5μm alignment tolerance of the available fabrication equipment. This longitudinal gap results to enhanced coupling losses, thus a fan-shaped PMMA taper section has been employed between the gold stripe and the silicon waveguide for coupling loss reduction purposes.

Characterization measurements were performed in order to evaluate the Si-to-DLSPP coupling losses as well as the straight DLSPP waveguide propagation losses. For this purpose, a dedicated cutback section was utilized, consisting of three sets of samples, each one comprising three DLSPP waveguides of 60, 80 and 100μm length, respectively. The fiber-to-fiber losses were measured employing a tunable Continuous Wave (CW) laser as input signal and a power meter. The TM-polarization state of the input signal was ensured with the use of polarization controller set prior to the chip's input. The wavelength tunability of the CW allowed for loss measurements directly at the resonance frequency of the grating couplers, avoiding any wavelength induced losses.

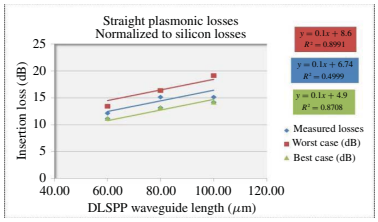

Fig. 3. Cutback measurements on 60-, 80-, and 100-μm-long DLSPP waveguide samples.

Figure 3 shows the total power losses estimation derived from measurements taken from the three sets of the straight plasmonic waveguides, plotted against the waveguide length. The depicted values were normalized to the losses induced by the silicon-based parts, negating the effect of the SOI circuitry. By properly fitting the measured data, propagation losses of around 0.10 dB/μm were observed for DLSPP waveguides while on average Si-to-DLSPP coupling losses of around 3.37 dB per facet were estimated. Due to the high dispersion of these measurements ($R^2 = 0.5$) probably owing to different Si-to-DLSPP coupling alignment achieved among the different structures, linear fitting for the three best and the three worst measurements was also performed, keeping the DLSPP waveguide propagation losses fixed at 0.1dB/μm. In this case, the Si-to-DLSPP coupling losses vary from 2.45dB to 4.3dB per interface, yielding indeed enhanced statistical accuracy. The 1.35dB higher losses compared to [7] are in-line with theoretical expectations [4] and owe mainly to the different SOI waveguide geometry used, which has been selected in our case so as to be compatible with fabrication of silicon-based passive functional circuitry.

III. Experiment and Results

The functionality of the chip's structures was evaluated both in terms of data transmission performance as well as of thermo-optic operation. The thermo-optic performance of the plasmonic structures was evaluated through the characterization of the all–pass racetrack ring resonator depicted in Fig. 1(b). A tunable CW laser was used to scan a spectral window of 80nm, ranging from 1500nm to 1580nm. This signal was used as input to the plasmonic ring resonator that exhibited 12dB losses at 1545nm. Current injection was enabled by utilizing electrical tips placed on the gold pads of the device. Step-by-step measurements of the output power were taken by scanning through the full range of the tunable laser initially without employing current, for reference purposes, and later for 50mA current. The respective spectral

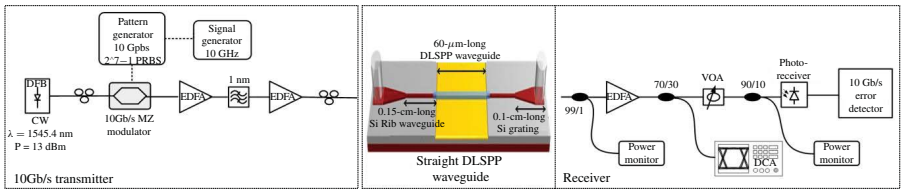

Fig. 4. Experimental setup of the 10-Gb/s transmission experiment through the straight DLSPP waveguide.

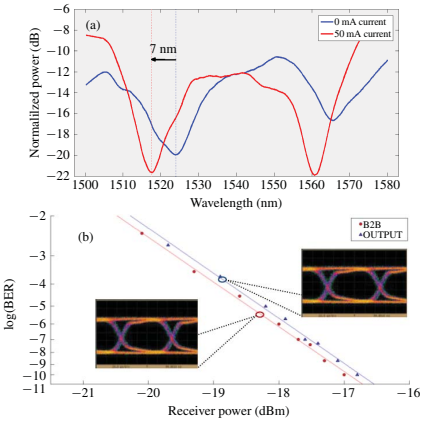

Fig. 5. (a) Spectral response of racetrack ring resonator over the range of 1500–1580 nm. (b) BER measurements and eye diagrams of the B2B and the output signal transmitted though the 60-μm Si-DLSPP waveguide.

responses were reconstructed by plotting the values of the output power versus the wavelength steps.

Following this, the transmission performance of the 60μm long plasmonic waveguide shown in Fig. 1(b) was assessed in a 10Gb/s transmission experiment. The experimental setup that was used for the evaluation process is depicted in Figure 4. A CW signal at 1545.4nm was launched into a Ti: LiNbO3 MZ modulator driven by a Pseudo-Random-Bit-Sequence (PRBS) pattern generator, yielding a 10Gb/s 2^7-1 NRZ data sequence at its output. The signal was then amplified by an Erbium-Doped-Fiber-Amplifier (EDFA) chain, providing 24dBm output, and launched into the plasmonic waveguide. The data signal at the output of the plasmonic waveguide was amplified and fed into a high–sensitivity Photo-Receiver connected to a 10Gb/s Error Detector in order for Bit Error Rate (BER) measurements to be performed.

Figure 5(a) shows the characterization results of the thermo-optic tuning of the racetrack ring resonator in the range of 1500 to 1580nm for two current injection states. The blue line represents the spectral response of the device for 0mA injected current (COOL state) while the red line corresponds to the spectral response that is obtained for 50mA injected current (HOT state). The simultaneous shifting of the two resonances suggests thermo-optic tuning of the device by 7nm towards smaller wavelengths, owing to the negative sign of the thermo-optic coefficient of PMMA [7]. This wavelength shift yields an extinction ratio of 8dB at 1561nm between the HOT and COOL states of the device, corresponding to an induced temperature change of 61K and consuming only 3.3mW of electrical power. Returning, however, to the initial state of the ring resonator, after switching off current, was not achieved, implying that the reversibility of the device was lost, most probably due to heating it above the maximum service temperature of the PMMA strip [7]. It becomes clear though that better results could be expected by exploiting a polymer strip which either exhibits higher thermo-optic coefficient than PMMA or is more tolerant to high temperature operation. The Q-value of the resonator was measured around 98 at "COOL" state and 142 at "HOT" state for the 1565nm and 1561nm resonant wavelengths, respectively, while its Free Spectral Range (FSR) value was 41.7nm when unheated.

Figure 5(b) shows the Bit-Error-Rate (BER) curves obtained for the 10Gb/s data transmission through the straight DLSPP waveguide. Error–Free operation was obtained for the transmitted signal with a power penalty of less than 0.2dB against the B2B measurements, implying no impact on the transmitted signal as confirmed by the eye diagrams at the inset.

IV. Conclusion

We have presented the first system-level experimental results of DLSPP structures hetero-integrated into a SOI chip. Experimental evidence of their data capture and signal integrity properties has been demonstrated by transmitting a 10Gb/s NRZ data signal through a 60μm long straight DLSPP waveguide, yielding error–free operation with negligible power penalty (<0.2dB). The low-energy thermo-optic tuning capability of the DLSPP-on-SOI platform has been also experimentally identified through the wavelength tuning of a plasmonic ring resonator over more than 7nm, consuming only 3.3mW of electrical power. The reported results denote the strong potential of the DLSPP waveguides aided by Si-Plasmonic hetero-integration towards the penetration of plasmonic technology in actual datacom applications.

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