

2x2 All-Optical Exchange-Bypass Switch

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Abstract We demonstrate an optically addressable 2x2 exchange-bypass switch operating with 10 Gbps data packets. Switching is achieved in an optical amplifier gate and the performance of the device is independent of packet length and content.

Introduction

In the quest towards high capacity data networks, all optical packet switching is set to provide a path for the deployment of more efficient transport networks [1]. Avoiding intermediate layers such as SDH and ATM is considered to be the solution to handle the growing Internet traffic and to provide a variety of optical services in an affordable way [2,3]. For optical packet switching, the optical layer must be transformed from a static transmission medium to a dynamically reconfigurable facility. This should possess the ability of changing the connectivity between nodes during the time scale of a packet and possibly to allow for some limited bit-wise processing. Towards this end, potential switch matrices based on semiconductor materials in guided wave structures, have been demonstrated [4-9]. Despite their impressive performance, these switches are best suited for long packets due to their slow switching speed compared to the bit period.

In this paper we present an optically addressable, semiconductor optical amplifier (SOA)-based 2x2 exchange-bypass switch operating at 10 Gbps. The switch operates successfully with data packets of arbitrary length and content and is appropriate for high-speed optical packet switching, time slot interchanging, add/drop multiplexing, packet header insertion/erasing and OCDMA. A concatenation of suitably synchronized switches could also serve as a traffic shaper for aggregating bursty Internet traffic and generating packet flows that utilize efficiently the time slot [7]. The switch is based on the Ultrafast Nonlinear Interferometer (UNI) gate [10-11], which has been shown to be capable of operation up to 100 Gbps [12].

Experiment

The switch principle of operation is illustrated in Figure 1 and the experimental setup is shown in Figure 2. The 2x2 exchange bypass switch consists of a SOA-based Ultrafast Nonlinear Interferometer (UNI) gate, which is configured to provide two signal inputs and two signal outputs. The Polarization Beam Splitter (PBS) at the input combines the two data signals in orthogonal polarization states for entry into the UNI gate. The

control signal is launched into the gate using a 80:20 fiber coupler in counter propagating direction to the data signals and is synchronized in bit level to the data signals. At the output of the switch and in the absence of the control signal, data signal 1 passes through port 1 while data signal 2 passes through port 2 of the PBS. The control signal causes the polarization state of each of the data signals to be rotated by 90° and as a result data signal 1 appears in port 2 while data signal 2 appears in port 1. The length of the bit sequence that is interchanged through the switch is determined by the length of consecutive 1's in the control signal and may be arbitrarily long or short depending on the incoming packet length. In the experiment proper synchronization between the control and data signals 1,2 was achieved with the variable optical delay lines ODL4 and ODL5.

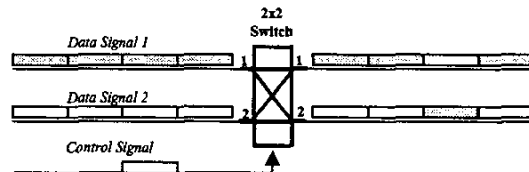


Fig. 1. Principle of operation

The switch was powered with two gain-switched DFB diode lasers, LD1 and LD2 that provide the data and control signals respectively. LD1 operates at 1549.2 nm and was driven from a synthesized signal generator at 1.25 GHz to produce 8.1 psec pulses after linear compression with DCF of total dispersion -54 psec/nm. The pulsetrain was then modulated in a LiNbO_3 modulator (MOD1) driven from a pseudorandom bit pattern generator to produce a 2^7-1 maximal length bit sequence at 1.25 Gbps. The bit rate was optically multiplied eight times in a split-relative-delay-and-recombine bit interleaver, which was constructed entirely from polarization maintaining (PM) fiber and components to ensure environmental stability. Data signal 1 was formed from the 10 Gbps maximal length pseudorandom bit sequence after being modulated in a LiNbO_3 modulator (MOD3) driven from a pulse generator to produce 2.5 nsec packets of bits with 6.4 nsec period. Data signal 2 was the full 10 Gbps PRBS with 12.8 nsec period. The control signal was generated

from LD2 at 1549.2 nm, which was driven from a synthesized RF signal generator at 10 GHz and produced 8.4 psec pulses after linear compression with DCF of total dispersion -47 psec/nm. This pulsetrain was then modulated in a LiNbO₃ modulator (MOD2) to produce control packets of 3.2 nsec duration and 6.4 nsec period. In this way data signals can be viewed as sequences of data packets with fixed length 3.2 nsec or 32 bits long while the control signal as a packet of 32 consecutive 1's with 3.2 nsec duration and a period of 6.4 nsec. The UNI gate uses a commercially available (Opto Speed S.A.), 1.5 mm bulk InGaAsP/InP ridge waveguide SOA with peak small signal gain of 30 dB at 1560 nm with 700 mA drive current.

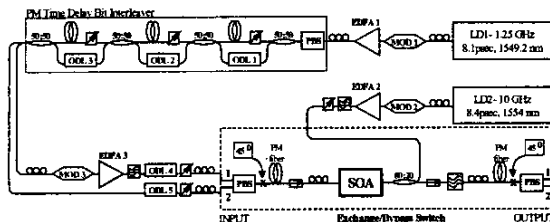


Fig. 2. Experimental setup

Results

The operation of the switch was successfully tested with this data input format and the results are shown in Figure 3 obtained on a 30 GHz sampling oscilloscope. Figures 3a and 3b show the bar state of the switch. Data packet 1 (thick dashed line) and data packet 2 (thin dotted line) enter and leave the switch at port 1 and 2 respectively. Figures 3c and 3d show the cross state of the switch. Data packet 1 (thick dashed line) enters the switch at port 1 and leaves the switch at port 2, while data packet 2 (thin dotted line) enters the switch at port 2 and leaves the switch at port 1. Figure 3e shows the control signal that is needed for the switch to exchange the data packets. The particular data formats for signals 1, 2 and control described above were chosen for easy visualization of the switch operation but the switch was shown to operate equally well with different packet formats. The pulse energy of the data 1, data 2 and control signal during the operation of the switch was 2, 2 and 8 fJ respectively. The crosstalk of the switch in the bar and cross states was -12 dB and -10 dB respectively. When the switch is in the exchange state there is also a 1dB drop in its transmission as a result of higher gain saturation of the SOA in the presence of the control signal, but this may be eliminated if a gain transparent arrangement is used [13]. The BER of the switch for both the bar and cross state was measured in the order of 10^{-11} . The rotation of the polarisation vector due to the polarisation gain dependence of the SOA as well as the PM fiber arrangement in the UNI resulted in the increase of

errors as the polarisation states of the interacting signals drifted. However simple adjustment of the polarisation controllers was sufficient for the switch to operate error-free.

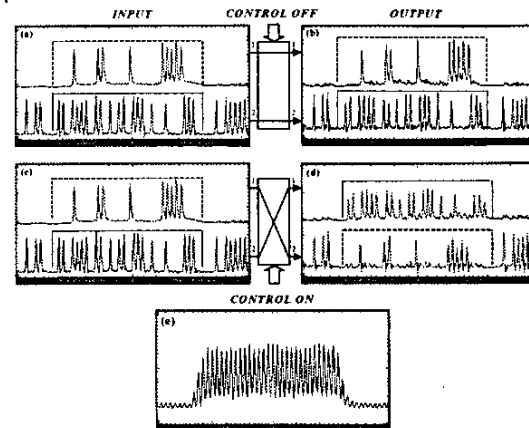


Fig. 3. Bar and cross state of the switch.

Conclusions

We have demonstrated a 10 Gbps optically addressable, 2x2 exchange bypass switch that may be used in optical packet switching applications. The switch requires low energy to operate and has been evaluated with different packet lengths and packet contents. The switch may operate with incoming data packets of the same or different wavelengths and its switching speed is expected to be scalable well beyond 40 Gbps. Active polarisation control could ensure the error free operation of the switch.

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