40 Gb/s Fast-Locking All-Optical Packet Clock Recovery

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Abstract: We demonstrate instantaneous 40 Gb/s clock extraction from 1 ns long data packets separated by 750 ps. The circuit comprises a Fabry-Perot filter and an all-optical power limiting gate and requires very short inter-packet guardbands.

OCIS codes: (060.2330) Fiber optics communications; (230.1150) All-optical devices; (250.5980) Semiconductor Optical Amplifiers; (050.2230) Fabry-Perot

1. Introduction and Concept

In order to satisfy the increasing demands for higher speed and more efficient bandwidth utilization, optical packet-switched network nodes should be designed to support transmission of closely-spaced short packet traffic at line rates beyond the currently available by electronic circuits. In this context, the subsystems that are destined to deal with the 3R regeneration, error-free reception and subsequent optical signal processing of the data within the node should be able to handle short data packets with minimum arrival time delays at line rates reaching 40 Gb/s. This, however, poses stringent requirements on all-optical node synchronization and local optical clock signal generation, requiring clock extraction on a per-packet basis without increasing bandwidth overheads. In this rationale, the performance metrics of such a packet clock recovery circuit is the clock acquisition time and clock persistence time. Ideally, to achieve maximum bandwidth utilization, a packet clock should be generated instantaneously and persist only for the duration of the incoming data packet.

So far, several all-optical clock recovery techniques suitable for packet-mode operation at 40 Gb/s have been proposed, including synchronized mode-locked ring-lasers [1], electronic phase locked loops [2] and self-pulsating DFBs [3]. Ring-lasers and phase locked loops require a large time interval for synchronization to the data streams and are most suitable for traffic in the form of large aggregated packets. Self-pulsating DFBs require significantly less overhead for clock acquisition and can operate successfully with data packets comprising of a few thousands of bits and guard bands of a few hundreds of bits.

In this communication we demonstrate a packet clock recovery circuit able to achieve instantaneous locking on 40-bit long packets at 40Gb/s requiring 2 preamble bits for clock synchronization. In addition the circuit exhibits a self-resetting time of only 16 bits drastically reducing the guardband overhead between packets. The configuration comprises a low-Q Fabry-Perot Filter (FPF) [4] tuned at the line-rate that due to its short impulse response allows for packet-to-packet processing. Exploiting the filter memory effects, the '0's of the incoming data stream are partially filled with preceding '1's creating a signal that resembles a packet clock but is amplitude modulated. A deeply saturated semiconductor optical amplifier (SOA) interferometric gate is then incorporated in order to remove the amplitude modulation by taking advantage of its thresholding function. The proposed circuit is self-synchronizing, data-format insensitive [5] and requires no high-speed electronics, whereas the lock-in time and the required intra-packet guardbands are limited to a small number of bits. Since these guardbands are packet length and bit rate independent and given that optical gates can operate beyond 100 Gb/s [6], the circuit has great potential for use in future high-speed and optically transparent OPS networks with enhanced transmission efficiency and bandwidth utilization.

2. Experimental Setup

The experimental setup is depicted in Figure 1 and consists of the optical packet generator and the clock recovery circuit. An actively mode-locked fiber ring-laser (MD-FRL) provided a 9.872 Gb/s pulse train consisting of 1.6 ps pulses at 1555 nm. This pulse-train was modulated to form a 2^7-1 PRBS signal using a PRBS generator and a Ti:$LiNbO_3$ modulator (MOD1) and was time-multiplexed in a polarization maintaining (PM) bit interleaver to generate a 39.488 Gb/s pseudo-data stream. Data packets of adjustable length and period were formed using a

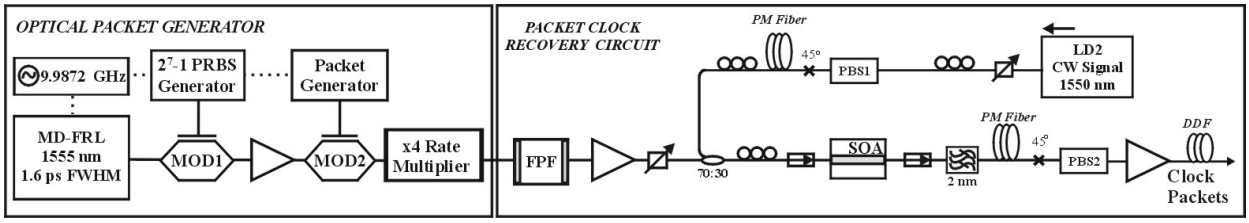

Fig. 1. Experimental setup.

second Ti:$LiNbO_3$ modulator (MOD2) driven by a programmable PRBS generator. The resulting packet stream was then launched into the packet clock recovery circuit, consisting of a low-Q FPF and a SOA-based UNI gate, powered by a CW signal at 1550 nm (LD2). The FPF played the role of the passive optical resonator that helps extracting the line rate spectral component and due to its short exponentially decaying impulse response the data packets are transformed into clock packets with intense amplitude modulation and duration similar to the corresponding data packets. The output of the filter was amplified and inserted into the UNI gate as the control signal. To help the fast recovery of the SOA, the UNI gate was optimized for operation at 40 Gb/s, using PM fiber that induces only 5 ps of birefringent delay in the two orthogonal polarization components of the CW signal at the input and output ports of the gate. The CW signal plays the role of an optical holding beam, further reducing the recovery time of the SOA [7], while its power was adjusted to deeply saturate the SOA and bias the interferometer in the saturated regime. The saturation of the nonlinear gate by the CW light injection, yields a power-limiting power transfer function [8], providing the intensity modulation reduction that is necessary for generating a packet-level clock signal. Finally, the self-extracted clock packets were amplified in an EDFA and fed into a Dispersion Decreasing Fiber (DDF)-based pulse compressor used at the output of the UNI gate. The FPF used was a bulk, micrometer-adjustable fused quartz substrate with free spectral range (FSR) equal to the line rate and finesse equal to 50. The active element in the optical gate was a 1.5 mm bulk InGaAsP/InP ridge waveguide SOA with 27 dB small signal gain at 1550 nm and a recovery time of 80 ps, when driven with 700 mA (OPTOSPEED S.A.).

3. Results and Discussion

Data packets of different length, period and content were used to evaluate the performance of the clock recovery circuit at 40 Gb/s. Fig. 2(a) shows a sequence of four, 40-bit long packets separated by 750 ps. Entering the FPF, the packet stream is convolved with the exponentially decaying response function of the filter, so that deeply amplitude modulated, but nevertheless clock resembling packets are obtained as shown in Fig. 2(b).

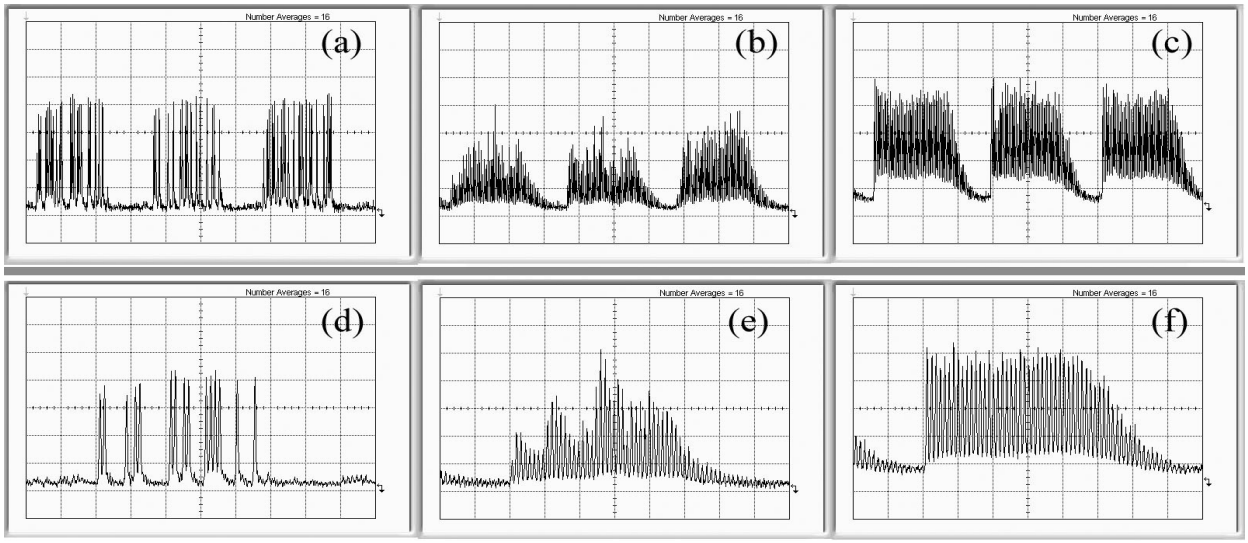

Fig. 2. (a), (b), (c) Input data packets, FPF output and recovered clock packets (time base 500 ps/div, vertical scale 335 μW/div) and (d), (e), (f) Single packet, FPF output and recovered clock (time base 200 ps/div, vertical scale 335 μW/div)

Introduction of this signal as control signal into the saturated UNI gate results in the generation of clock packets with very short rise and fall times as depicted in Figure 2(c). Figures 2 (d), (e) and (f) provide a more detailed view of a single packet, its form after passing through the FPF and its transformation to an amplitude equalized packet clock signal. More specifically Figure 2 (f) reveals that the clock is captured from the first bit and exhibits a fall time of 16 bits, whereas the amplitude modulation (highest to lowest pulse ratio) within the 40 clock pulses is below 1 dB. The sharp rise time is a result of the heavy saturation of the SOA and determines the lock acquisition time of the circuit, whereas the fall time is due to the lifetime of the filter and determines the minimum intra-packet guardbands. Successful operation of the circuit was achieved by injecting 1 mW of optical power from the CW signal and 80 fJ/pulse from the data signal.

The timing jitter performance of the circuit was investigated using a continuous PRBS signal at 40 Gb/s with the precision time base option of an Agilent/HP 86100A Infinium digital sampling oscilloscope. Figure 3 (a) and (b) show the eye diagrams obtained for the input signal and recovered clock respectively. The rms timing jitter for the input signal was measured to be 450 fs and 580 fs for the recovered clock. The slight increase in rms jitter measured was due to the difficulty of precisely aligning the bulk FPF used, resulting in small line-rate detuning. This effect can be eliminated by using a fiber-based FPF. The circuit was also sensitive to phase variations caused by the susceptibility of mode-locked fiber ring lasers to environmental changes. The autocorrelation trace obtained at the output of the circuit is provided in Figure 3 (c) to examine the pulse shape and temporal width of the optical clock pulses. The pulses have a temporal FWHM of 4 ps, whereas their hyperbolic secant profile can be verified by the ideal sech fit provided.

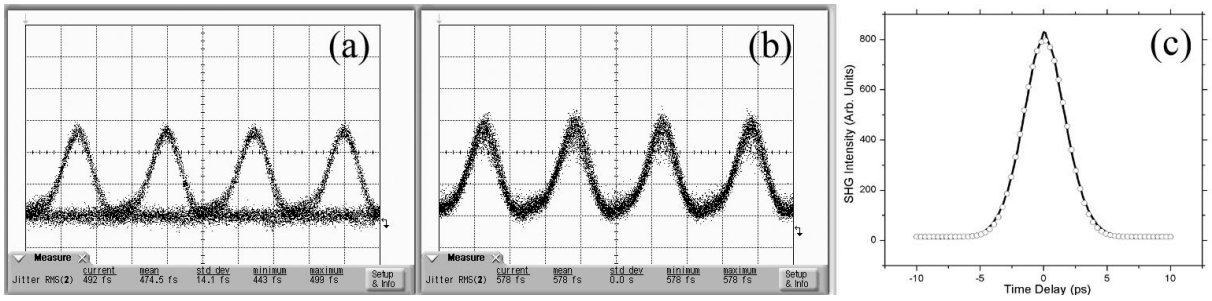

Fig. 3. (a), (b) Eye diagrams (100ps/div, 500 μW/div) of input data and extracted clock and (c) Autocorellation trace and sech fit of clock pulses.

4. Conclusion

We have presented all-optical clock recovery from short, 40 Gb/s data packets using a clock recovery circuit consisting of a low-Q FPF and a deeply saturated UNI gate. This scheme is based on simple optical filtering and switching elements, requires no high-speed electronics and provides improved bandwidth efficiency, since it instantly acquires synchronization on packets separated by short, sub-nanosecond inter-packet gaps.

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