# A 40 Gb/s 3R Burst Mode Receiver with 4 integrated MZI switches

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**Abstract:** We demonstrate for the first time a 40 Gb/s all-optical 3R burst-mode receiver error-free operation for 9,3 dB power fluctuation between short bursty packets. It consists of a sequence of four integrated MZI switches.

## 1. Introduction and Concept

Optical Burst/Packet Switching have been introduced as the main switching paradigms for the future IP-centric network traffic layers in order to exploit the inherent bursty nature of the data and provide increased bandwidth utilization and finer granularity to the network.3R Burst mode reception is typically completed in a three-stage procedure: power equalization of the incoming bursts, clock extraction and data recovery for every burst separately. To this end, a 3R burst mode receiver should possess a large dynamic range and ultra-fast response characteristics in order to properly handle variable length data packets irrespective of their power level and their synchronization. So far, mainly electronic 3R implementations have been reported [1] that require a few preamble bytes in order to achieve power equalization and phase recovery, with the most recent circuit operating at 10 Gb/s and exhibiting 9.2 dB power fluctuation tolerance [2]. All-optical attempts to perform successfully as burst mode receiver circuits have indicated the potential of photonic solutions to reach higher data rates, but have limited themselves to 2R characteristics [3].

In this article we demonstrate what we believe to be the first all-optical 3R burst mode receiver circuit operating with 40 Gb/s asynchronous, variable length bursts with intense power variation. The circuit is completely based upon hybridly integrated Mach-Zehnder Interferometric Switch technology. It employs a record of four cascaded MZIs each one performing a different functionality. The first MZI acts as a power equalization element [4], the second one operates as a wavelength converting adaptive interface and the remaining two MZIs with the aid of a Fabry-Perot filter perform clock and data recovery, respectively [5]. The demonstrated circuit exhibits 9,3 dB dynamic range, has a lock-in time of only 5 bits and requires 14 bits as inter-packet guardbands. The proposed technique requires no high-speed electronics, has great potential for use at the receiver end of high-speed and data transparent Optical Burst/Packet Switched networks with enhanced transmission efficiency and bandwidth utilization.

## 2. Experimental Setup

The experimental setup is shown in Fig.1. It consists of the 40 Gb/s asynchronous packet flow generator, an array of four hybrid integrated MZIs (HMZI) forming the burst mode receiver (BMR) and an additional HMZI used as a 40 to 10 Gb/s demultiplexer. The BMR comprises a power equalization unit (PE) implemented by an unbalanced HMZI, an adaptation interface based on a HMZI in a wavelength conversion configuration and the clock and data recovery unit (CDR) that employs a fiber Fabry-Perot filter and two cascaded HMZIs performing clock recovery and data reception, respectively. Towards forming the asynchronous packet traffic, a 1553 nm DFB laser was gain switched at 10.025 Gb/s to produce 7 ps pulses after linear compression. This pulse train was launched into a non linear fiber pulse compressor to reduce its pulse width to 3 ps. After exiting the compressor, it passed through a Ti:LiNbO$_3$ electro-optic modulator driven by a 10.025 Gb/s pattern generator and was multiplexed to 40.1 Gb/s in a fiber bit-interleaver to form a $2^7$-1 PRBS data pattern. The output of the multiplexer was launched into a second modulator driven by an electronic pulse-pattern generator to produce data packets of unequal lengths. This packet stream was then introduced in the asynchronous split-and-delay packet flow generator that consists of a 3 dB coupler with fiber lengths at its output, to provide 250 ns of differential delay between the two paths before

recombination in a second 3 dB coupler. The burst-mode traffic obtained at the output of the asynchronous packet flow generator entered then as the input signal the HMZI that performs the power equalization functionality.
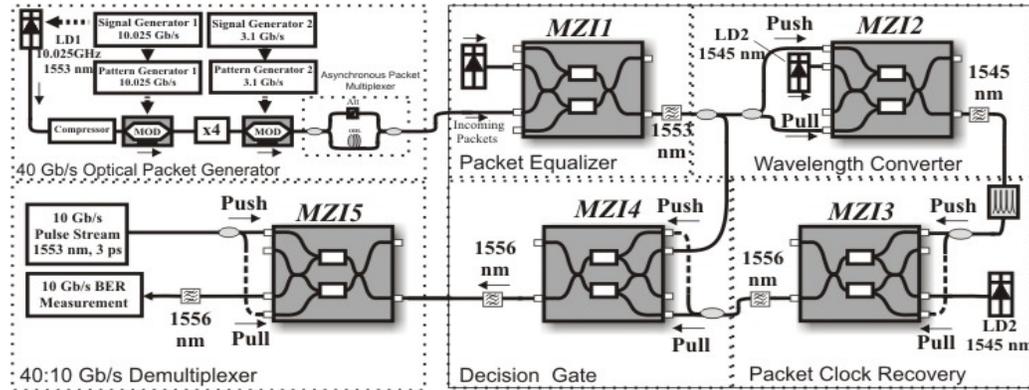


Fig. 1. Experimental Setup

This HMZI was configured to provide a self-switching operation exploiting its unbalanced coupling ratios (70/30) and the different SOA driving conditions. In this way, the intensity modulated input signal was power equalized at the output of the two SOAs taking advantage of the different SOA gains exhibited by the weak and the strong packet, respectively. Moreover, the different gain saturation due to the different SOA driving currents (340 mA and 190 mA, respectively) induces also a differential phase shift between the signals traveling through the two HMZI branches, which in turn leads to interference between these signals at the output of the HMZI. As such, a combination of the unbalanced HMZI transfer function and the different SOA gain dynamics at each branch results in power equalized output packets without increasing the noise level. This novel application of the HMZI device required xx fJ of the input signal to operate successfully, whereas 150 uW of a counter-propagating CW signal were also used to accurately adjust the gain levels of the SOAs.The power equalized packet stream was then split and the one part was fed as the control signal into *MZI2* to perform wavelength conversion and clock recovery, whereas the other part entered as input signal the *MZI4* for data reception. The wavelength conversion stage acts as an adaptive interface to assign locally controlled signal parameters for the wavelength, carrier phase and power stability to the incoming signal, providing at its output a 40 Gb/s data signal at 1558 nm with a pulse width of 7 ps. This wavelength converted signal entered the clock recovery module that consists of a fiber Fabry-Perot filter (FFP) having a FSR of 40.1 GHz and a finesse of 39, followed by an additional HMZI (*MZI2*) powered by a CW signal at 1556 nm (LD2) and operating as a power limiter [CR]. Data reception was completed in *MZI4* by using the power equalized packets as input and the respective recovered clock packets as triggering signal, reducing in this way the timing jitter and the amplitude modulation of the input signal [CDR]. Finally, bit error rate (BER) measurements were performed after demultiplexing the 40 Gb/s packets into 10 Gb/s data streams using *MZI5* as a demultiplexer. *MZI5* was operated in push-pull control configuration with 3 ps clock pulse stream at 1553 nm used as the control signal.

### 3. Results and Discussion

By changing the width, period and delay of the electrical pulse train driving the second modulator, data packets of various length, period and contents were generated in order to test the performance of the BMR circuit. Fig. 3 illustrates the evolution of the burst mode reception process through trace and eye diagrams obtained at each stage of the circuit. Fig. 3(a) shows a typical sequence of four asynchronous incoming data packets at 40 Gb/s having a size of 48 and 75 bits, respectively, and exhibiting power fluctuation of 9.3dB. BER measurement for the input signal is shown in Fig. 4, where error free operation was measured for no power fluctuation. Fig. 3(b) shows the respective power equalized packet stream obtained at the output of *MZI1*. The 9.3 dB power fluctuation between the incoming packets has been reduced into roughly 3dB amplitude modulation between the pulses within the power equalized packets, while the noise '0' level remains unaffected. BER shows that error free operation is possible, but for increased input power to the receiver. Figure 3(c) depicts the wavelength converted data signal exhibiting a moderate improvement regarding the amplitude modulation. Figure 3(d) shows the recovered clock packets obtained at the output of the clock recovery stage. They are ensuring clock persistence for duration equal to that of

the corresponding data packets increased by 5 bits at its beginning and 14 bits at its end. The former value indicates the time required by the clock recovery to lock to the line-rate of the incoming data packet, as shown in the inset of this figure, while the latter value determines the time required by the CR signal to decay to 1/e after each packet. Figure 3(e) illustrates the received equalized data packets at the output of the burst mode receiver, indicating clearly that timing jitter and amplitude modulation reduction with respect to the corresponding signal at the output of the power equalization unit (*MZI1*) is obtained. BER measurement shows a negative power penalty of 1,95 dB for the received packets.
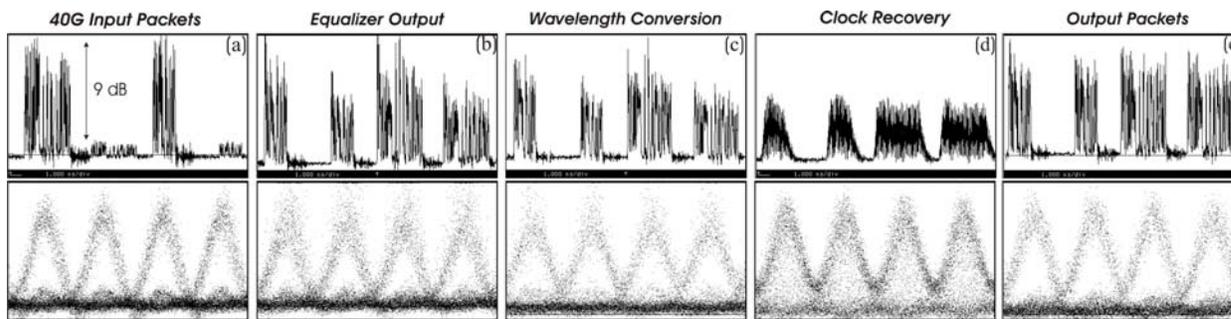


Fig. 2. Traces and eye diagrams for input, equalization unit, wavelength conversion, clock recovery and output signals
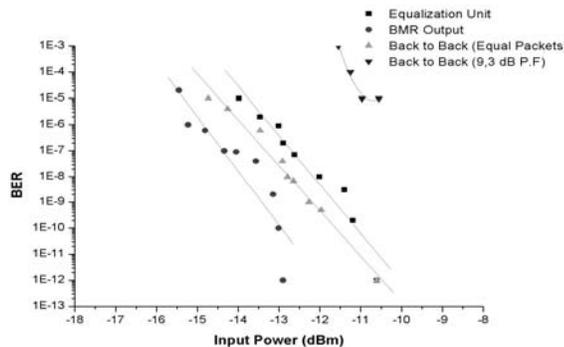


Fig. 2. BER measurement for input signal, after equalization state and output.

## 4. Conclusion

We have presented an all-optical burst mode receiver operating at 40 Gb/s and capable at equalizing 9,3 dB of packet to packet fluctuations. The setup was implemented using a sequence of four integrated MZI switches, showing the capability for multiple all-optical gate operations.

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