All-Optical Four-Wavelength Burst Mode Regeneration Using Integrated Quad SOA-MZI Arrays


Abstract—We demonstrate an all-optical four-wavelength 3R burst mode regenerator, operating error-free with 10-Gb/s variable length data packets that exhibit 6-dB packet-to-packet power variation. The circuit was implemented using a sequence of three integrated quadruple semiconductor optical amplifier-based Mach–Zehnder interferometric arrays.

Index Terms—Burst mode regenerator (BMR), dynamic range, hybrid integrated Mach–Zehnder interferometer (HMZI), optical burst switching, optical packet switching, wavelength-division multiplexing (WDM), optical time-division multiplexing (OTDM).

I. INTRODUCTION

Recent statistics on current global traffic have recorded a capacity increase which exerts pressure on the deployed wavelength-division-multiplexing (WDM) networks. Even though the insertion of additional wavelengths to the existing infrastructure seems to satisfy the present demands, this solution does not seem adequate for the near future [1]. Efforts are now focusing on increasing the network’s transparency through the use of all-optical techniques and by increasing the transmission rates to 40 Gb/s or even 100 and 160 Gb/s per channel. The adaptation of these solutions, however, is strongly dependent on the development of multifunctional, multiwavelength and compact photonic components that can perform advanced network functionalities [2]. Following this rationale, specific attention has been given to the integration of semiconductor optical amplifier-based interferometric optical gates [(SOA)-Mach–Zehnder interferometers (MZIs)] as the key technology for the implementation of photonic signal processing circuits due to their fast response [3] and integrability into compact, switching units [4]. Single-element integrated SOA-MZIs have been thoroughly investigated and verified in field trials [5], whereas currently the integration of arrays of SOA-MZIs and their demonstration in multigate experiments are revealing the great potential of photonic technology in optical networking [6]. So far, the potentials of multigate integration have become evident mainly in single-wavelength time domain applications. However, the path to successful exploitation of these devices in all-optical networks lays in the successful interconnection of multiple arrays and their successful operation in demanding hybrid WDM/optical time-division multiplexing (OTDM) applications such as multiwavelength regeneration and wavelength routing.

In this letter, we present the simultaneous operation of three, hybrid integrated quad SOA-MZI arrays (HMZI), comprising a total amount of 12 integrated photonic optical gates and demonstrate an all-optical four-wavelength burst mode regenerator (4 λ-BMR). The BMR system performs power equalization and 3R regeneration (retiming, reshaping, and reamplification) of variable length return-to-zero (RZ) data packets. Each one of the three SOA-MZI quad arrays performs a different functionality in the 4λ-BMR architecture: 1) power equalization, 2) clock recovery (CR), and 3) regeneration of the incoming packets. Each quad array accommodates four wavelength operation of this functionality. The circuit performed error-free with 10-Gb/s variable length RZ data packets, showing a negative power penalty up to 2.5 dB for the recovered data channels in respect to the corresponding input data channels with 6-dB power fluctuation.

II. EXPERIMENT

The experimental setup of the 4 λ-BMR is shown in Fig. 1. It consists of the 10-Gb/s optical packet generator, the power equalization unit, implemented with the first quad HMZI array, the CR circuit which employs a Fabry–Pérot filter (FPF) in combination with the second quad HMZI array and the data recovery circuit, implemented with the third quad HMZI array. Four continuous-wave (CW) signals at 1554.94, 1556.55, 1558.17, and 1559.79 nm were multiplexed and inserted into an electroabsorption modulator (EAM), producing 6-ps RZ pulses at 10.0229 GHz at its output. This pulse train was then fed into a Ti : LiNbO₃ electrooptical modulator driven by a 10.0229-Gb/s pattern generator, to produce 2⁷⁻¹ pseudorandom binary sequence (PRBS) format data packets of unequal lengths. The data packets were then inserted into a second Ti : LiNbO₃ modulator, driven by a 78-MHz low rate signal generator, to create 6-dB packet per packet power fluctuations. A 1 × 4 AWG was used to separate the four wavelengths, which were then entered as inputs into the first quad array of the 4 λ-BMR circuit. In order to achieve the power equalization process of the incoming data channels, each wavelength served as an input to one of the four HMZI switches of the quad. The HMZIs of the first quad had unequal splitting ratios (60/40) and were
configured to self-switch the incoming packet traffic, by also using different current values for their two SOAs [7]. With this arrangement, the saturation properties of the two SOAs resulted in high gain for the low power packets and low gain for the high power packets, delivering nearly power equalized packets at the outputs of the HMZIs. The power equalized data packets at the output of the first array were multiplexed and split into two parts. One part was fed to the CR circuit, whereas the other part was fed as a control signal into the third quad HMZI switch for the data reception. The CR employed a low-Q fiber FPF with free spectral range equal to the line rate (10.0229 GHz) and a finesse of 47, followed by the HMZIs of the second quad array [8]. Each HMZI of the second quad array was powered by a CW signal corresponding to the following configuration: 1558.17 nm for Q2-HMZI3, 1559.79 nm for Q2-HMZI4, 1554.94 nm for Q2-HMZI1 and 1556.55 nm for Q2-HMZI2. The four wavelengths at the output of the FPF were separated with the use of a 1×4 AWG and each one served as a control signal to one of the four HMZI switches of the second quad. In order to reduce the switching window of the HMZIs, both control ports of each gate were used. By properly adjusting the relative time delay and powers of the two control signals (push–pull configuration), a reduction of the gates’ switching window was achieved [10], resulting in the extraction of 8-ps clock pulses at their outputs. Data reception was completed in the HMZI switches of the third quad array, by using the power equalized packets as switching signals and their corresponding recovered clock packets as inputs, reducing in this way the timing jitter, and the amplitude modulation of the input signal [8], [9]. The timing jitter of the input data has been mainly due to the timing jitter of the signal generator used to drive the EAM. Push–pull control configuration was also adopted in the HMZIs of the third array. Finally, bit-error-rate (BER) measurements were performed for all four data channels. The SOA bias currents were 190 and 270 mA for each one of the HMZIs of the first quad HMZI array and 300 mA for the other two HMZI switches. The switching powers were 4 and 0 dBm for the push and pull control signals of the HMZIs that operated as power equalizers in the second array and 1 and −4 dBm, respectively, for the HMZIs of the third array. Isolators and polarization controllers were used between the HMZI stages to stop backward propagating noise and signals and to adjust polarization of the input signals. Erbium-doped fiber amplifiers were also used in order to compensate the losses between stages of the 4λ-BMR circuit.

III. RESULTS AND DISCUSSION

Data packets of different length were used for the experimental validation of the 4λ-BMR circuit. Fig. 2 illustrates the evolution of the burst mode regeneration process through temporal oscilloscope traces and eye diagrams obtained at each stage of the 4λ-BMR circuit. Fig. 2(a) shows two incoming data packets at 10 Gb/s having a length of 119 and 60 bits, respectively, and exhibiting power fluctuation of 6 dB. Fig. 2(b) shows the respective power equalized packet stream obtained at the outputs of the HMZIs of the first quad array. The 6-dB power fluctuation between the incoming packets has been reduced into roughly 1-dB amplitude modulation between the pulses within the power equalized packets. Fig. 2(c) depicts the recovered clock packets obtained at the output of the CR stage. They persist for time duration that equals that of the corresponding input data packet, extended on its leading edge by a 4-bit rising time and on its trailing edge by a 16-bit decay time. The former value indicates the time required by the CR to lock to the line-rate of the incoming data packet, while the latter value determines the time required by the CR signal to decay to 1/e after each
Fig. 2. Experimental results of the 4λ-BMR circuit. Trace and eye diagrams of (a) incoming 6-dB power fluctuated packets, (b) power equalized packets, (c) packet CR, and (d) regenerated data packets. Trace and eye-diagram time scales are 1 ns/div and 10 ps/div, respectively.

Fig. 3. Experimental results for BER measurements.

We have presented an all-optical four-wavelength 3R BMR operating error-free with 10-Gb/s data packets of variable length and 6-dB packet per packet power fluctuation. Error-free operation was obtained with negative power penalties for all outputs of the circuit. The circuit was implemented using a sequence of three integrated quad HMZI arrays showing the functional and performance capability offered by multiple all-optical gates.

IV. CONCLUSION

We have presented an all-optical four-wavelength 3R BMR operating error-free with 10-Gb/s data packets of variable length and 6-dB packet per packet power fluctuation. Error-free operation was obtained with negative power penalties for all outputs of the circuit. The circuit was implemented using a sequence of three integrated quad HMZI arrays showing the functional and performance capability offered by multiple all-optical gates.

REFERENCES