All-Optical Packet Address and Payload Separation

C. Bintjas, N. Pleros, K. Yiannopoulos, G. Theophilopoulos, M. Kalyvas, H. Avramopoulos, and G. Guekos

***Abstract*—An all-optical address and data separation scheme is presented for short 10-Gb/s packets. The technique uses a novel packet clock recovery circuit that consists of a Fabry–Pérot filter and a ultrafast nonlinear interferometer (UNI) gate to generate a local packet clock. A second cascaded UNI gate is used to separate the header and the payload, performing a simple AND operation between the packet and its self-derived clock. The proposed technique requires a small number of bits as guard band and this number is independent of the line rate.**

***Index Terms*—Address extraction, nonlinear interferometer, optical routing, optical signal processing, packet switching, semiconductor optical amplifier (SOA), ultrafast nonlinear interferometer (UNI).**

I. Introduction

THE REMARKABLE advances in lightwave technology of the past decade have succeeded in reducing vastly, the long distance, point-to-point transmission cost. Optical packet switching concepts are being introduced as the means toward extending this benefit beyond point-to-point transmissions and fully exploiting bandwidth capacity at the network level [1], [2]. Toward this goal all-optical techniques are expected to assist in releaving the network from undesirable latencies related to O/E/O conversions at the switching nodes, especially assuming that transmission line rates will continue to increase beyond 10 Gb/s. In order to transmit packets from source to destination all-optically, it is crucial to be able to generate local clock signals for processing, as well as to be able to separate and recognize the address information embedded in a packet. In an effort towards all-optical routing, several techniques have been proposed so far for the all-optical separation of address from payload [3]–[7]. In these methods synchronization is achieved either with high speed electronics [3] or with optical switching and time multiplexing, self-synchronization schemes that generate the local clock signals powering the optical gates performing the address separation task, for the duration of the address part of the packet [4]–[7]. Even though these methods have demonstrated the potential of all-optical processing, their circuit complexity increases with the number of header bits.

In this letter, we demonstrate a simple optical circuit that can separate all-optically, the address from the payload of 10-Gb/s optical packets. The circuit consists of two units: a recently demonstrated packet clock recovery circuit [8] that generates an optical clock signal persisting for the duration of the packet and a high-speed ultrafast nonlinear interferometer (UNI) optical gate [9], [10] that uses this clock signal to separate header and payload with a logical AND operation. The packet clock recovery unit uses a Fabry–Pérot (FP) filter to partially fill the "0s" of the incoming packet, followed by a UNI gate to equalize their amplitudes. Important features of the technique presented here for the header and payload separation are that the circuit does not make use of any high-speed electronics and that only the 10-Gb/s optical packet is needed as input for the separation task to be performed. Finally, the circuit requires only a small number of bits as guard band between packets. This guard band is related to the finesse of the FP filter and does not depend on the line rate.

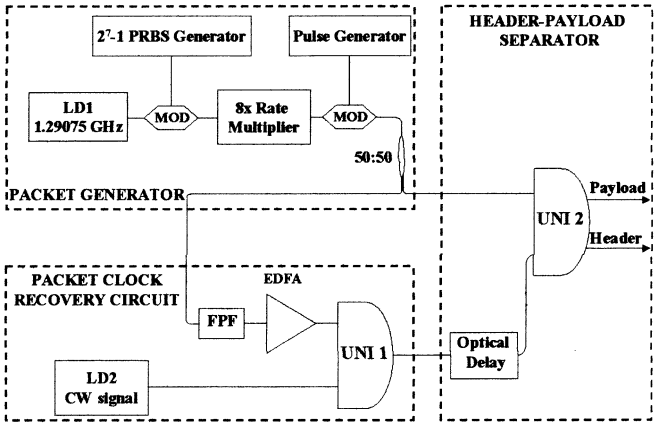

Fig. 1. Block diagram of the all-optical address and payload separation circuit.

II. Concept and Experiment

Fig. 1 shows the block diagram of the circuit with the optical packet generator, the clock recovery and the address and data separation units. The optical packets were generated using a distributed-feedback (DFB) laser diode (LD1), which was gain switched at 1.29075 GHz to provide 8-ps pulses at 1549.2 nm after linear compression in a dispersion compensating fiber of total dispersion -96 ps/nm. This pulse train was modulated with a $2^7 - 1$ pseudorandom binary sequence (PRBS) pattern in a $Li:NbO_3$ modulator and was three-times bit interleaved to generate a pseudodata pattern at 10.326 Gb/s. Data packets of different length and period were produced using a second $Li:NbO_3$ modulator driven from a programmable pulse generator.

The output of the packet generator circuit was divided into two parts, one used in the packet clock recovery circuit and the second used for the address/payload separation. The packet clock recovery unit consists of a FP filter and a UNI gate. The optical signal was fed into the FP filter that has free spectral range (FSR) equal to the line rate and finesse equal to 20.7. The

Manuscript received May 22, 2002; revised July 26, 2002.

C. Bintjas, N. Pleros, K. Yiannopoulos, G. Theophilopoulos, M. Kalyvas, and H. Avramopoulos are with the Department of Electrical and Computer Engineering, National Technical University of Athens, GR 15773 Athens, Greece (e-mail: cbint@cc.ece.ntua.gr).

G. Guekos is with the Swiss Federal Institute of Technology Zurich, ETH Hoenggerberg, CH-8093 Zurich, Switzerland.

Digital Object Identifier 10.1109/LPT.2002.804654

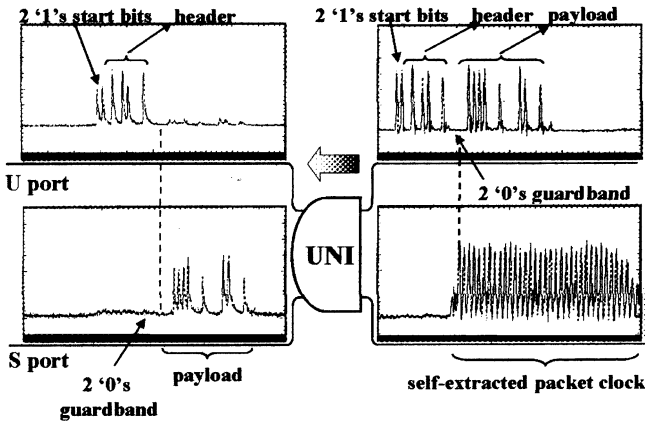

Fig. 2. Principle of operation of header/payload separation.

impulse response function of the filter is a decaying exponential function with lifetime defined by its finesse [11], so that if an RZ modulated data signal is introduced in the FP the "0s" in the incoming stream become partially filled by preceding "1s" at its output. The large amplitude modulation of this clock resembling signal may be removed in a nonlinear UNI gate (UNI 1), if it is used as the switching control signal in the gate that is powered by the continuous-wave (CW) signal from a second DFB laser (LD2), in this instance at 1545 nm [8]. The active nonlinear element of UNI 1 was a commercially available (Opto Speed S.A.), 1.5-mm bulk InGaAsP–InP ridge waveguide semiconductor optical amplifier (SOA) with 27 dB small signal gain at 1550 nm, 24 dB at 1545 nm and a recovery time of 100 ps, when driven with 700-mA current. The control signal was brought in counterpropagating direction from the CW signal in the SOA, so as to cause a differential phase change of about π between the two orthogonal polarization components of the CW signal and to result in a nearly equal amplitude clock signal with duration approximately equal to that of the original packet. The UNI operated as an AND gate and was biased so that with no optical control signal, the CW signal appeared in its unswitched port U, while in the presence of control pulses the signal appeared in its switched port, S. During operation the clock packets are extended at their leading and trailing edges due to the lifetime of the FP filter. However due to the saturation properties of the SOA, the rise of the leading edge of the packet clock signal is much shorter than its decay time or the lifetime of the FP. In the front of the packet, the SOA is less saturated and can provide higher gain to the first bits, so that even these low energy pulses can cause enough phase shift on the CW component.

Address and payload separation was performed in a second UNI gate (UNI 2) built identically to UNI 1 and configured so as to perform an AND operation between the original packet signal and the recovered packet clock. The principle of operation of our scheme is detailed in Fig. 2. Successful header extraction is performed if the original packet and the packet clock are synchronized at the input of UNI 2, so as to have a time delay equal to the duration of the address. The packet clock is delayed in an optical delay line for a time duration equal to the packet address, so that only the bits forming the payload of the original packet fall within the window of the recovered clock and are switched in the gate. In this way the payload appears in the S-port of UNI 2 and the address in its U-port. In order to assist the clock extraction process and due to the short but nonzero rise time of the packet clock circuit, a number of "1s" are required at the leading edge of the packet. Also, in order to avoid switching with the first imperferct bits from the clock circuit, an equal number of "0s" is required between the header and the payload and finally due to the noninstantly decaying clock, a fixed guard band is needed between two packets. The three packet formatting requirements are a result of the storage property of the FP filter and are defined by its finesse. The channel bandwidth overhead associated with these requirements, is reduced if packets with smaller header to payload ratios are used.

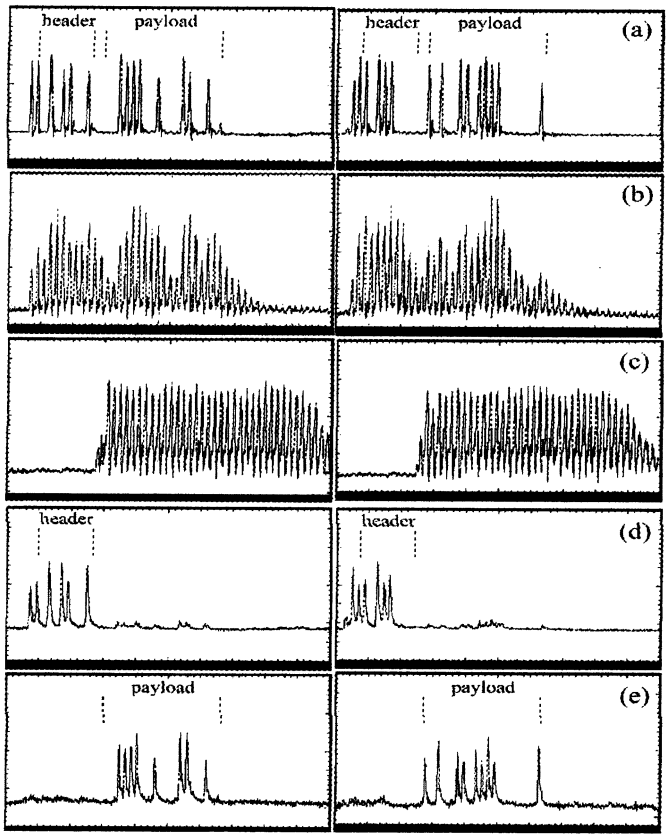

Fig. 3. (a) Typical data packets. (b) Corresponding output from the FP filter. (c) Recovered and delayed packet clock. (d) Packet address at U-port. (e) Packet payloads at S-port of UNI 2. The time base is 500 ps/div.

III. Results and Discussion

Data packets of different length, period and content, were used to test the performance of the header extraction system at 10-Gb/s nominal rate, by changing the width, period and delay of the electrical pulse driving of the second modulator. Fig. 3(a) shows typical results for two such packets, containing 30 bits, with approximately 3-ns duration arriving at 6.2-ns intervals. For this case and with a FP of finesse 20.7, the rise time of the packet clock recovery circuit was 2 bits and its 1/e fall time was 8 bits. As a result the packets shown here were formatted to contain two "1s" as preamble bits, 8 bits assigned to header, a guard band of two "0s" and finally 18 bits for the payload. For example the header of the first packet consists of "0 1 0 1 1 0 0 1," while its payload of "0 0 1 1 1 1 0 0 1 0 0 0 1 1 0 0 1 0."

Fig. 3(b) illustrates the corresponding outputs of the FP etalon showing the clock resembling but highly amplitude modulated signal. The FPF introduced 12-dB losses in the incoming data. Fig. 3(c) shows the self-extracted clocks for the two packets at the output of UNI 1 and appropriately delayed for the AND operation with the packets of Fig. 3(a). This figure shows that UNI 1 has reduced the amplitude modulation of the clock pulses to 1.5 dB, the packet clock rises within 2 bits and that it falls to 1/e within 8 bits. Switching power and mean energy per pulse for the CW and the control signal were 1 mW and 120 fJ, respectively. These two parameters determine the degree of saturation of the SOA and enable the control pulses to affect a differential phase change of roughly π between the two polarization components of the CW signal in the UNI.

To complete the header/payload separation task the properly synchronized packet and self-extracted clock signals are logically ANDed together in UNI 2. Fig. 3(d) and (e) show respectively separated, the headers and payloads of the packets at the U and S-ports of UNI 2. The pulse energies for the signals interacting in UNI 2 were 2 fJ for the data pulses and 24 fJ for the packet clock pulses. Note the difference in switching energies between the first and second gate, the reason being that the SOA in UNI 1 must be deeply saturated to remove the amplitude modulation of the clock resembling output from the FP filter. The gain in UNI1 between packet clock at the output and input packet was about 4 dB. In UNI2 the gain for the payload and header parts of the packet between output and input was about 4 and 7 dB. The average contrast ratio between the ON–OFF states of UNI 2 at the output of the circuit was 8 : 1 for the payload (S-port) and 6 : 1 for the header (U-port). The data patterning seen in Fig. 3 is primarily due to imperfect rate multiplication and can be largely eliminated if a 10-Gb/s transmitter source is used.

The packet formatting requirements discussed before are a result of the finesse of the FP filter, which must be optimized in terms of the expected sequence of continuous "0s" in the header and payload of the incoming data packets against amplitude modulation, rise and fall times. Simulations have shown that the clock recovery circuit may handle data streams with up to 30 consecutive "0s" with a FP of finesse 80, retaining its very sharp rise time of a few bits, but a longer decay time [8]. It should also be noted that the rise and fall times of the clock recovery circuit are defined by the finesse of the FP as fixed numbers of bits and are independent of the rate. Therefore assuming that optical switching is possible in excess of 100 Gb/s [9], this technique should be in principle extendable to higher rates, without enforcing an increase in the number of bits in the guard bands. Finally, with the technique described here the circuit complexity does not increase with the length of the header. For packets with different address length, one has to alter the temporal delay between the optical signals at the input of UNI 1.

IV. Conclusion

In conclusion, we have presented all-optical address and data separation for short optical packets at 10 Gb/s. The data packets self-extract their clock in a novel packet clock recovery circuit, which consists of a FP filter and a UNI gate. The address and the payload of the packet are separated in a second UNI gate, which performs an AND operation between the properly delayed clock and packet signals. The circuit is simple, has no high-speed electronic or active optical units and minimizes the guard bands between packets to a small number of bits. Instead of using bulk components as demonstrated here, the circuit should be easily integrable or at least may be built using a fiber FP filter and integrated and polarization insensitive gates of the Mach–Zehnder type [12] for increased simplicity and ease of use.

Acknowledgment

The authors would like to thank R. Dall'Ara and S. Hansmann of Opto Speed, S. A. for providing the SOA and DFB lasers.

References

[1] M. J. O'Mahony *et al.*, "The application of optical packet switching in future communication networks," *IEEE Commun. Mag.*, vol. 39, pp. 128–135, Mar. 2001.

[2] C. Guillemot *et al.*, "Transparent optical packet switching: The European ACTS KEOPS project approach," *J. Lightwave Technol.*, vol. 16, pp. 2117–2134, Dec. 1998.

[3] T. J. Xia *et al.*, "All-optical packet-drop demonstration using 100 Gb/s words by integrating fiber-based components," *IEEE Photon. Technol. Lett.*, vol. 10, pp. 153–155, Jan. 1998.

[4] M. C. Cardakli *et al.*, "Reconfigurable optical packet header recognition and routing using time-to-wavelength mapping and tunable fiber Bragg gratings for correlation decoding," *IEEE Photon. Technol. Lett.*, vol. 12, pp. 552–554, May 2000.

[5] K. Chan, F. Tong, C. K. Chan, L. K. Chen, and W. Hung, "An all-optical packet header recognition scheme for self-routing packet networks," in *Proc. OFC*, Paper WO4, pp. 284–285.

[6] D. Cotter *et al.*, "Self-routing of 100 Gbit/s packets using 6 bit 'keyword' address recognition," *Electron. Lett.*, vol. 31, pp. 1475–1476, 1995.

[7] K.-H. Park, T. Mizumoto, A. Matsuura, and Y. Naito, "All-optical address extraction for optical routing," *J. Lighwave Technol.*, vol. 16, pp. 1129–1136, July 1998.

[8] C. Bintjas *et al.*, "Clock recovery circuit for optical packets," *IEEE Photon. Technol. Lett.*, vol. 14, pp. 1363–1365, 2002.

[9] K. L. Hall and K. A. Rauscenbach, "100-Gbit/s bitwise logic," *Opt. Lett.*, vol. 23, pp. 1271–1273, 1998.

[10] C. Bintjas *et al.*, "20 Gb/s all-optical XOR with UNI gate," *IEEE Photon. Technol. Lett.*, vol. 12, pp. 834–836, July 2000.

[11] X. Zhou *et al.*, "A performance analysis of an all-optical clock extraction circuit based on Fabry–Pérot filter," *J. Lightwave Technol.*, vol. 19, pp. 603–613, 2001.

[12] T. Fjelde *et al.*, "Demonstration of 20 Gb/s all-optical logic XOR in integrated SOA-based interferometric wavelength converter," *Electron. Lett.*, vol. 36, pp. 1863–1864, 2000.