ALL-OPTICAL ADDRESS AND DATA SEPARATION FOR 10 Gb/s PACKETS

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Abstract *We present all-optical address and data separation for 10 Gb/s cells. The technique uses a novel packet clock recovery circuit to generate the local signal and an optical gate to extract header and payload.*

Introduction

During the last decade, lightwave technology has become the vehicle for the realization of inexpensive point-to-point transmission bandwidth and optical packet switching concepts are being introduced to fully exploit bandwidth capacity at the network level [1]. All-optical techniques are expected to assist in optical packet switching as they may releave the network from latencies related to O/E/O conversions. In order to transmit information from source to destination all-optically, it is crucial to be able to generate local clock signals for processing as well as to be able to separate and recognize the address information embedded in a packet. So far several all-optical techniques have been proposed for address extraction [2-6]. The majority of these methods employ optical logic gates and time multiplexing synchronization schemes to generate local clock signals to power the gates for the duration of the address part of the packet. Even though these methods have demonstrated the potential of all-optical techniques, they are address-format-specific and their circuit complexity increases as the number of header bits is increased.

In this presentation we show a simple optical circuit that can separate all-optically, the address from the payload of 10 Gb/s optical packets. The circuit consists of two units: a novel packet clock recovery circuit [7] that generates an optical clock signal of approximately equal length to the packet and a high speed UNI optical gate [8-10] that uses this clock signal to separate header and payload with a logical AND operation. The packet clock recovery unit uses a Fabry-Perot filter to partially fill the '0s' of the incoming packet, followed by a UNI gate that equalizes their amplitudes. An important attribute of our technique is that it does not require any high speed, electronic or active optical subsystem, so that only the 10 Gbps optical packet is needed as input for its header and payload to be separated.

Experimental Setup

Fig.1 shows the experimental setup with the block diagram of the optical packet generator, the clock

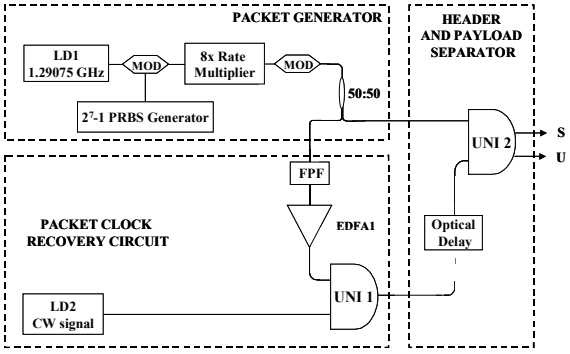

Figure 1 Experimental Setup

recovery and address and data separation circuits. The optical packets were generated using a DFB laser diode gain switched at 1.29075 GHz to provide 8 ps pulses at 1549.2 nm after linear compression. This pulse train was modulated with a 2^7-1 PRBS pattern in a Li:NbO_3 modulator and was 3-times bit interleaved to generate a pseudo-data pattern at 10.326 GHz. Finally data packets of different length and period were produced using a second Li:NbO_3 modulator.

On entering the address and data separation circuit, the packets were divided in two parts. The first part was fed into the Fabry-Perot filter of the clock recovery circuit [7], with FSR equal to the line rate and finesse equal to 20.7. The output of the filter was used as control signal in UNI 1, which was powered with a CW signal from a second DFB laser at 1545 nm and which was used to equalize the amplitude after the Fabry-Perot and to generate the packet clock. The active element of UNI 1 was a 1.5 mm bulk InGaAsP/InP ridge waveguide SOA with 30 dB small signal gain at 1560 nm and a recovery time of 100 ps, when driven with 700 mA current. The second part of the packet signal enters the second, UNI 2 gate and is switched using the recovered packet clock signal from UNI 1. Successfull header extraction can be performed if the packet clock and original packet are synchronized in UNI 2 so as to have a time delay equal to the duration of the address, as shown in Fig. 2. To ensure this process, in our example the packets comprise of two '1's as start bits to assist the clock

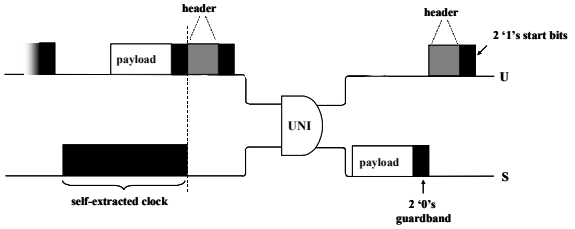

Figure 2 Principle of operation

extraction [7], 8 bits assigned to header, a guardband of two '0's to avoid switching by the first two imperfect bits at the leading edge of the clock and finally 18 bits for the payload. UNI 2 was set to perform a logical AND and the data bits were switched to the S-Port, while the address bits appeared at the U-Port.

Results

Data packets of different length, period and content, were used to test the performance of the system at 10 Gb/s nominal rate. Fig. 3 shows typical results for two such packets (fig. 3(a), (a')), containing 30 bits, with approximately 3 ns duration arriving at 6.2 ns intervals. Note, for example, that the first packet consists of header "0 1 0 1 1 0 0 1 and payload "0 0 1 1 1 1 0 0 1 0 0 0 1 1 0 0 1 0". It also includes two '1's as start bits and two '0's between header and payload due to the characteristics of the clock extraction process. Figs. 3(b), (b') illustrate the self-extracted clocks for the two packets, respectively, as they appear at the output of UNI 1 and timed correctly for header/data separation. The modulation of the clock

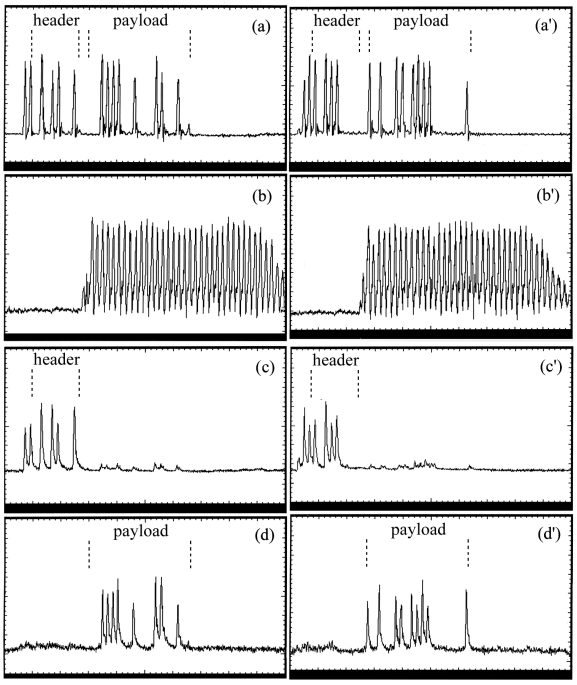

Figure 3:(a), (a') Typical data packets, (b), (b') corresponding recovered packet clock at exit of UNI 1, (c), (c') packet address at U-port and (d), (d') packet payloads at S-port of UNI 2. The time base is 500 ps/div.

pulses was less than 1.5 dB, and the rise time was only 2 bits.

Synchronized in this way, the packet and self extracted clock signals are logically ANDed together in UNI 2 for header/payload separation. Figs. 3(c) and (c') show the headers at one output port of UNI 2 (the U-port) including the two start-bits and figs. 3(d) and (d') show their corresponding payloads at the other port (S-port) of the gate. The pulse energies for the signals interacting in UNI 2 were 2 fJ for the data pulses and 24 fJ for the packet clock pulses. The contrast ratio between the ON-OFF states of the switch was up to 10:1 for the S-port and 8:1 for the U-port and the pulses comprising the optical packet retained their pulse width. It should be noted that the complexity of this configuration does not depend on the duration of the header. For packets with different address length, one has to alter the temporal delay between the optical signals at the input of UNI 1.

Conclusions

In conclusion, we have presented all-optical address and data separation for short optical packets at 10 Gb/s. The data packets self-extract their clock in a novel packet clock recovery circuit, which consists of a Fabry-Perot filter and a UNI gate. The payload of the packet is switched in a second UNI gate which performs an AND operation between clock and packet. The circuit is simple, has no high-speed electronic or active optical units and minimizes the guardbands between packets into a few bits, a number defined by the lifetime/finesse of the Fabry-Perot filter. Given that the lifetime of the filter is defined as number of bits and that the UNI gate has been shown to operate in excess of 100 Gb/s, this circuit should be capable of operation at comparable rates retaining its short guardband requirements even at the higher line rates.

References

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