All-optical clock recovery from short, asynchronous data packets at 10 Gb/s

N. Pleros, K. Vyrsokinos, C. Bintjas, K. Yiannopoulos, K. Vlachos, H. Avramopoulos and G. Guekos

***Abstract*— In this paper, we demonstrate clock extraction from 10 Gb/s asynchronous short data packets. Successful clock acquisition is achieved from data packets arriving at time intervals of only 1.5 ns, irrespective of their precise phase relation. The clock recovery circuit used consists of a Fabry-Perot filter (FPF) and a non-linear UNI gate and requires very short time for synchronization.**

***Index Terms*— Burst mode, clock recovery, optical packet/burst switching, Ultrafast Nonlinear Interferometer-UNI, Semiconductor Optical Amplifier-SOA**

I. Introduction

Optical packet switching has been introduced as the main concept to overcome limitations related to O/E/O conversions and to fully exploit bandwidth capacity, especially as it offers distinguishing advantages such as on-demand use of bandwidth and the ability to switch bursty traffic [1]. However, the lack of a simple and reliable optical memory that can store and retrieve the information bit by bit as well as the bursty nature of the traffic profile, imposes the need for dynamically switched optical nodes that are capable to handle asynchronous packets from different sources on their way to different destinations [2],[3]. In order to manage efficiently such short, asynchronous optical packets, it is crucial to be able to extract asynchronously the clock signal on a packet-by-packet basis.

Several techniques have been proposed for all-optical clock recovery, including synchronized mode-locked ring-lasers [4], electronic phase locked loops [5] and self-pulsating DFBs [6],[7]. Ring-lasers and phase locked loops require a long time for synchronization to the data streams and are not suitable for asynchronous, short optical packet traffic. Self-pulsating DFBs require significantly less overhead for clock acquisition and have been demonstrated to operate successfully with asynchronous data packets comprising of a few thousands of bits and guard bands of a few hundreds of bits [6], at rates up to 40 Gbps [7]. Recently, we have demonstrated a novel clock recovery circuit that acquires clock, within a few (2) bits, from short (30-bit long) packets [8] and which for this reason can in principle reduce the guard band overhead between packets. This circuit was also used in a proof-of-principle experiment to demonstrate all-optical header from payload separation [9]. The circuit uses a low-finesse FPF followed by a semiconductor optical amplifier (SOA) - based Ultrafast Non-linear Interferometer (UNI) [10],[11]. The FPF is used to partially fill the '0's in the incoming data stream from the preceding '1's and to create a signal that resembles the packet clock but is amplitude modulated, while the UNI is used to remove this amplitude modulation.

In the present communication we show that the Fabry-Perot filter/UNI gate clock recovery circuit can acquire clock from asynchronous data packets at 10 Gbps, as would be encountered in the receiver of a 'real-life' node. To underline the capability of the circuit we use short (41 bits long) test packets and show for the first time to our knowledge clock acquisition from asynchronous packets, arriving at time intervals of as short as 1.5 ns between them. The proposed circuit is self-synchronizing, requires no high-speed electronics and can find applications in burst mode, packet receivers or all-optical signal processing circuits.

II. Experiment

Fig.1 shows the experimental configuration that consists of two main subsystems; the asynchronous packet flow

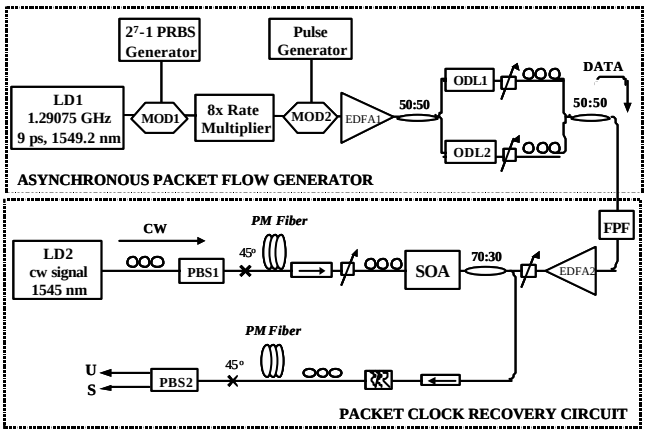

Fig. 1. Experimental Setup

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generator and the packet clock recovery circuit. A gain-switched DFB laser (LD1) at 1.29075 GHz, provided 9 ps pulses at 1549.2 nm after linear compression. This pulse-train was modulated with a 2^7-1 PRBS signal from a pattern generator and a $LiNbO_3$ modulator (MOD1) and was 3-times bit interleaved to generate a 10.326 Gbps pseudo-data stream. Data packets of variable length and period were formed using a second modulator (MOD2) driven from a programmable pulse generator. The packet stream was amplified in EDFA1 and split into two different optical paths via a 3 dB fiber coupler. The two paths were made so as to provide a maximum of 17.9 ns relative delay between the split signals. Polarization controllers and attenuators were used to independently adjust the polarization state and power in the two branches. Variable optical delay lines ODL1 and ODL2 were also used to independently control the relative arrival time of the packets at the clock recovery circuit, so as to investigate the minimum acceptable delay between successive packets and to assess the circuit ability to operate with successive packets that are asynchronous at the bit level. The asynchronous packet stream was then launched into the packet clock recovery circuit, which consists of a FPF and a UNI gate, powered by a CW signal at 1545 nm (LD2). The FPF had a free spectral range (FSR) equal to the line rate and a finesse of 20.7, corresponding to a 1/e lifetime roughly of 7 bits. The output of the filter was amplified in EDFA2 and inserted into the UNI gate as the control signal. The UNI gate was optimized for operation at 10 Gbps and used polarization maintaining fiber (PMF) at the input and output ports of the SOA to induce 50 ps of differential delay between the two orthogonal polarization components of the CW signal. The active element was a 1.5 mm bulk InGaAsP/InP ridge waveguide SOA with 27 dB small signal gain at 1550 nm, 24 dB at 1545 nm, 3 dB polarization gain dependence and a recovery time of 100 ps, when driven with 700 mA dc current. After exiting the SOA, the polarization components of the CW signal were filtered in a 2 nm filter, had their relative delay removed and were made to interfere in PBS2. The interferometer was biased so that, in the absence of the control signal, the CW signal appeared at its unswitched port, U, while in the presence of the control it appeared at its switched port, S.

III. Results and Discussion

Data packets of different length, period and content were used to evaluate the performance of this clock recovery scheme for asynchronous packet stream at 10 Gb/s. Fig. 2(a) shows a typical data stream, obtained from the asynchronous packet flow generator. More specifically, a sequence of four data packets is illustrated, each packet containing 41 bits (approximately 4 ns duration). Packets #1 and #3 are traveling through the upper and packets #2 and #4 are traveling through the lower branch of the packet generator. The coarse relative delay between packets #1 and #2 was 1.5 ns and between packets #2 and #3 2.9 ns. Packets #2 and #3 are shown in more detail in Fig. 3(a) and (b) respectively.

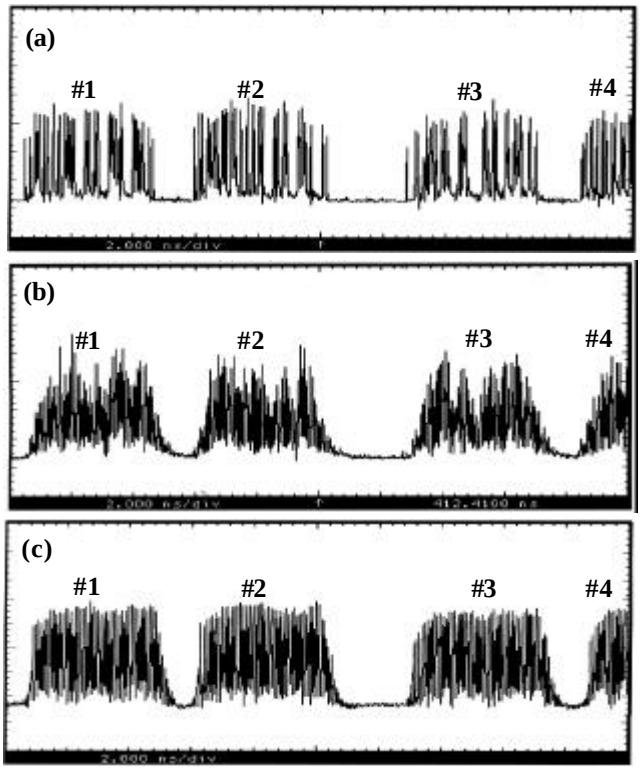

Figure 2 (a) Incoming asynchronous data stream of four packets and corresponding (b) FPF output and (c) recovered packet clocks. The time base is 2 ns/div.

At the FPF the asynchronous packet stream is convolved with the exponentially decaying response function of the filter, so that an amplitude modulated, but clock resembling signal is obtained. Fig. 2(b) shows the corresponding output of the FPF for packets #1 –to– #4. This is used as the control signal into the UNI gate to induce an almost p-phase shift between the orthogonal polarization components of the CW signal. This results in a packet clock signal of nearly equal amplitude '1's and very short rise and fall times. Fig. 2(c) shows the acquired packet clock signal. More detailed representation of the recovered packet clocks for packets #2 and #3 is illustrated in Fig. 3(c) and (d).

The packet clocks display rise and fall times of 2 and 8 bits respectively and amplitude modulation of less than 1.5 dB

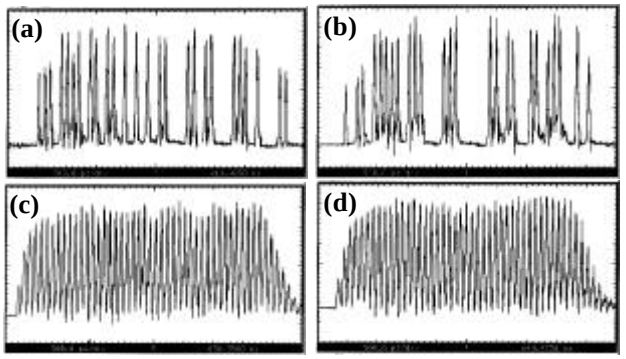

Figure 3: (a), (b) Detailed representation of two incoming data packets and (c),(d) corresponding recovered packet clocks. The time base is

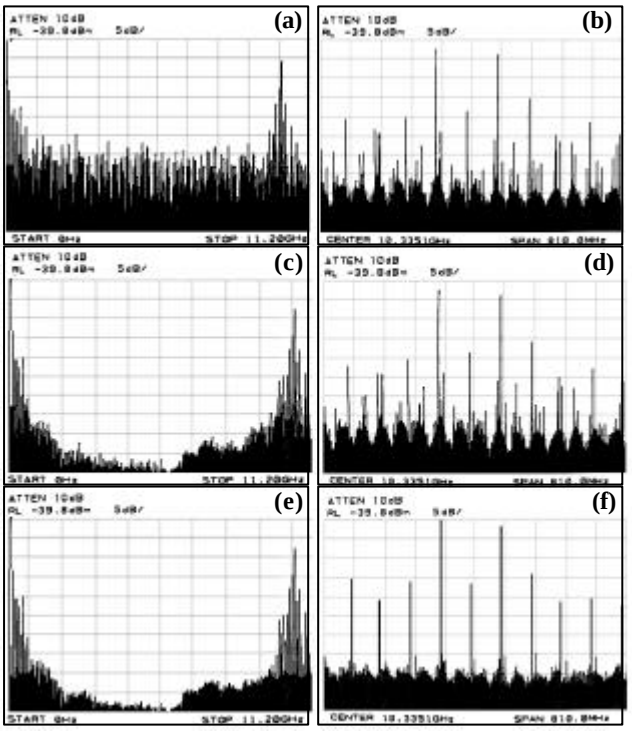

Figure 4: RF spectrum of (a) incoming asynchronous data packets, (b), (c) corresponding FPF output and (d) recovered packet clock. The span in (a), (b) is from DC-11.2 GHz and in (c) and (d) the centre frequency is around 10.326 GHz and the span is 810 MHz. The

(highest to lowest pulse ratio), within the span of the original 41 bit data packet. The circuit required 1 mW of optical power from the CW signal and 110 fJ/pulse from the data signal, corresponding to 0.9 mW average power for the packets shown here. Packet clocks of the same quality were obtained irrespective of the precise relative phase adjustment between the packets as set by the delay lines ODL1 and ODL2.

The quality of the asynchronously extracted clock signal was also examined using a 50 GHz microwave spectrum analyzer. Fig. 4(a) and (b) depict the RF spectrum of the packet signal from DC to 11.2 GHz and within a 810 MHz band centered around the 10.326 GHz component, respectively. The asynchronous operation is confirmed by the suppressed clock component at 10.326 GHz with respect to the adjacent 80 MHz spaced packet sub-harmonics. Fig. 4(c) and (d) show the corresponding output of the FPF. The effect of the filter is primarily to suppress all data modes outside a 500 MHz band around the base line rate. Data mode suppression within this 500 MHz band is achieved by taking advantage of the non-linear transfer function of the deeply saturated SOA-based interferometric gate [8]. Fig. 4(e) and (f) show the RF spectrum of the extracted packet clock at the output of the UNI gate for asynchronous traffic revealing data mode suppression in excess of 35 dB with respect to the 80 MHz spaced packet sub-harmonics. Finally, the rms timing jitter of the extracted clock was also calculated using the microwave spectrum analyzer for a total span of 3 KHz around the packet clock components and resolution bandwidth of 10 Hz, and was found to be less than 1 ps.

It should also be noted that the amplitude ratio between the 10.326 GHz clock component and the packet sub-harmonics has the same value in Fig. 4(b), (d) and (f), showing that the extracted clock retains the phase alignment of the initial asynchronous data stream. This amplitude ratio varies between a maximum value and zero, depending on whether the packets are perfectly phase aligned or misaligned by p, and this adjustment is provided by the setting of ODL1 or ODL2 within a bit-period time interval, approximately 100 ps.

IV. Conclusion

In conclusion, we have presented all-optical clock recovery from short, asynchronous 10 Gb/s data packets, arriving at time intervals of only 1.5 ns between them, by using a clock recovery circuit consisting of a FP filter and a UNI gate. The scheme requires no high-speed electronics, is self-synchronizing and would be suitable for packet routing with all-optical techniques [12],[13], even in the asynchronous traffic regime. To achieve polarization independence, simplicity and compactness, the circuit could be implemented using a fiber FP filter and UNI gates constructed with low polarization dependence SOAs or polarization insensitive gates of the Mach-Zehnder type. Even though the circuit was demonstrated with 10 Gb/s packets, it is expected that its speed should be extendable to significantly higher rates since the CW signal plays the role of an optical holding beam [14] and helps to reduce the recovery time of the SOA.

V. Acknowledgments

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