The European ICT-BOOM project: Photonic Tb/s routers made of silicon

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Abstract: BOOM aims at "siliconizing" photonic routers to enable ultra-high bit rates as well as higher levels of integration and power efficiency. Here we present the BOOM photonic routing device concepts based on silicon waveguide substrates.

Keywords: photonic routers, optical signal processing, wavelength conversion, hybrid integration, silicon-on-insulator, micro-ring resonators.

Introduction

Power efficiency in Telecommunication Networks is a key issue for the development of the next generation telecom hardware. The energy saving checklist includes broadband core networks, which now appear to be significantly energy hungry, since electronic carrier routing systems consume and dissipate large amounts of electrical power and heat respectively.

The turn towards photonic technology has initiated considerable R&D investments with the development of switching systems that prove the potential of integrated optics in efficient data routing. The focus is specifically on the fabrication of a chip-scale router that will enable Tb/s switching through mm-scale photonic chips as well as graceful scaling to Pb/s capacities keeping down cost and footprint. To this end, monolithic InP and hybrid multi-element photonic integration have been evolved in order to mark the transition from single element all-optical switches to large scale photonic processing systems on-chip. The most recent significant R&D highlights that outline this transition include:

- the 2x8 wavelength switch developed within DARPA funded project IRIS [1]
- the quadruple arrays of hybrid integrated SOA-MZI all-optical wavelength converters (AOWCs) developed within EU funded project MUFINS [2]
- the eight parallel SOA-MZI AOWCs integrated in InP within DARPA funded project LASOR [3].

Figure 1 shows how these achievements are now forming a new trend in functional photonic integration. From 2004 and on the upgrade path involves doubling the throughput of photonic routing devices every two years, whereas the current state-of-the-art photonic device is offering 320 Gb/s throughput on a small chip size of 4.25 x 14.5 mm^2 [3].

In order to keep up with this emerging trend and allow for even smaller, faster, cheaper and "greener" optical routing chips, a photonic integration platform that will enable scalable, functional and cost effective integration is required. Issues that are currently on the "photonic agenda" include thermal management within the photonic devices, further reduction of power consumption and – possibly - cost-effective fabrication with CMOS compatible technologies.

The European BOOM project [4] aims to create this technology by advancing the silicon-on-insulator (SOI) platform and provide highly integrated photonic router building blocks. InP to silicon bonding techniques and CMOS compatible waveguide fabrication will be key drivers in overcoming integration technology roadblocks and impact the development and deployment of the new transmission and switching equipment.

In this paper we describe the fabrication and device concepts of the project that officially set off on May 2008 and will conclude on April 2011. The ultimate goal is the development of the first silicon photonic wavelength routing prototype that will be capable to switch four 160 Gb/s line-rate channels, consume power equal to some 10s of Watts and occupy space as small as a 4 U rack-mount case.

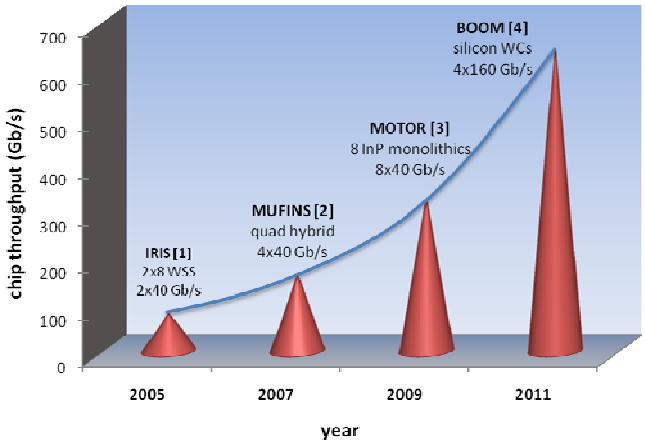

Figure 1 : Evolution of integrated optical processing systems

2. The BOOM concept

2.1 System overview

Figure 2 shows an artistic view of the BOOM wavelength routing concept. The BOOM platform incorporates the following parts:

- an array of AOWCs: the array incorporates a single active component (SOA) per AOWC followed by

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integrated filtering elements to realize chirp-filtering based all-optical wavelength conversion.

- an UDWDM photodetection unit: this consists of a compact micro-ring resonator demultiplexer followed by an array of 10 GHz integrated detectors. The component is used to filter out and detect the optical label of an incoming optical packet. The main challenge is to achieve a channel spacing as low as 0.1 nm with sufficiently low crosstalk in order to allow for a large number of attached optical labels and therefore a large number of ports in the photonic router. The detected labels are then processed by an electronic controller to generate the control signals.
- an array of integrated electro-absorption modulated lasers (EMLs): this consists of EMLs that are used to perform E/O conversion of the electronic control signals. As such the electronic control signals that are generated by the router controller are used to gate the EAM and a packet-length optical signal is generated to power the AOWC.

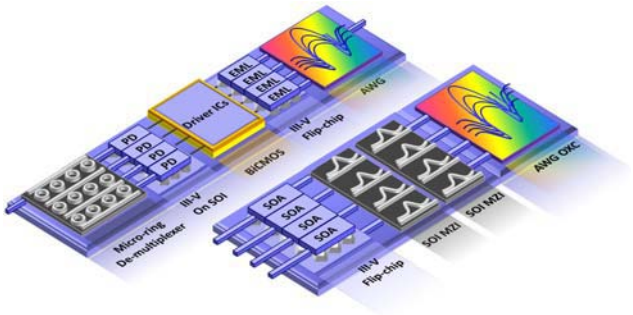

Figure 2: artistic view of the BOOM routing concept

In the following sections we outline the basic device layouts and the basics of the fabrication processes that are employed for the development of the BOOM silicon photonic components.

2.2 Hybrid integrated silicon photonic AOWCs

Figure 3a) shows an artistic view of the BOOM silicon photonic AOWC. The device incorporates two monolithic integrated periodic filters and a hybrid integrated SOA. The SOA is used to induce chirp in the converted probe signal due to the refractive index modulation caused by the pulsed pump signal. The first cascaded periodic filter is slightly detuned with respect to the probe wavelength and by filtering the blue (fast) chirp the acceleration of the effective recovery time of the system is achieved. The second filter is employed to restore the polarity of the optical pulses. Both periodic filters are implemented as passive MZI structures, integrated using SOI rib waveguide technology on substrates with a top silicon layer of 4um. The SOA can be flip-chip bonded on the same SOI board using AuSn or Sn/AgCu solder bumps.

The 4um waveguide substrate can guarantee efficient on-chip coupling of the pre-fabricated active component (SOA) as well as low loss pigtailing to lensed fibers during the packaging process. Figure 3b) shows the layout of the passive SOI part of the AOWC (device design by BOOM partner ICCS/NTUA). This involves two cascaded MZIs with differential delays of 1 and 2 ps respectively yielding a free spectral range (FSR) of 8 and 4 nm respectively. The measured spectral responses of both filters are illustrated in figure 3b). With this configuration a high-speed optical packet can be converted on any of the CW wavelengths that coincide with the “spectral comb” of the periodic filtering structure. Figure 3c) shows the first monolithic integrated SOI MZI AOWC platform mounted on a probe station (fabrication by BOOM partner TU Berlin).

Figures 3d) - e) show physical layer modeling results of the BOOM wavelength conversion scheme at 160Gb/s. Figure 3d) shows the eye diagram at the output of the SOA revealing the slow recovery time of the amplifier when 160Gb/s data are injected as pump signal. Figure 3e) shows the eye diagram at the output of the first detuned SOI MZI that indicates the effective recovery time of the system within the 160Gb/s bit slot. Figure 3f) shows the eye diagram at the output of the second SOI MZI indicating the successful pulse polarity inversion.

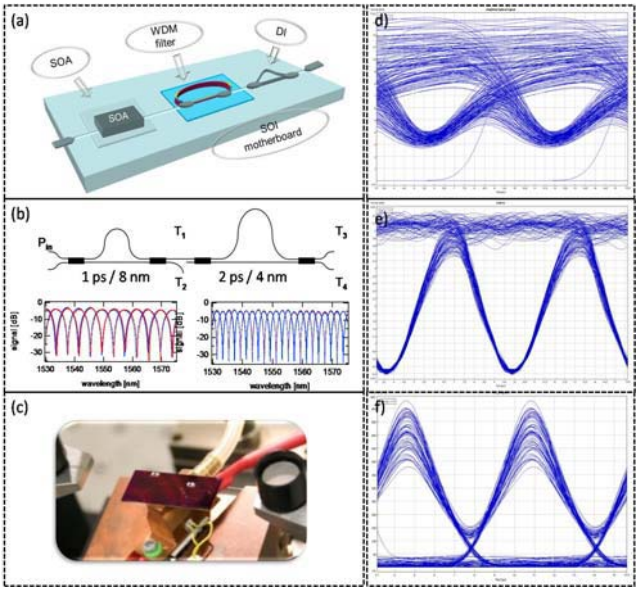

Figure 3: a) schematic view of the BOOM AOWC device concept, b) layout and measured responses of passive SOI MZIs, c) monolithic integrated SOI MZI AOWC platform. Modelling results at 160 Gb/s : d) SOA output, e) output of first MZI, f) output of second MZI

Figure 4a) and b) show the first pump probe measurements using a pigtailed SOA and the SOI chip at 40 Gb/s (measurements by BOOM partner TU/e). Figure 4a) shows the inverted signal at the output of the SOA indicating the slow recovery time of the amplifier. Figure 4b) reveals that the SOI-MZI filtering accelerates the operational speed of the system within the 40 Gb/s bit slot as well as restores the polarity of the optical pulses.

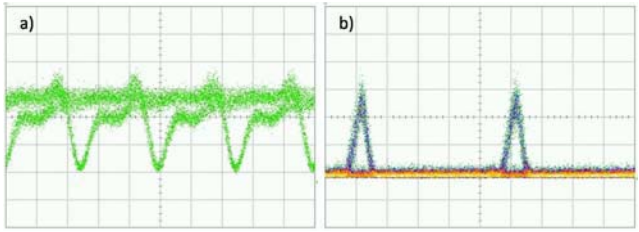

Figure 4: Pump-probe measurements at 40 Gb/s : a) SOA output, b) SOI MZI chip output. Time scales : a) 10 ps/div and b) 5 ps/div

2.3 Hybrid integrated silicon photonic photodetectors

Figure 5a) shows a schematic view of the UDWDM photodetector component. The device incorporates an UDWDM demultiplexer implemented with eight cascaded SOI nanowire micro-ring resonators and eight hybrid integrated evanescent photodetectors integrated on the same chip. Figure 5b) illustrates the SEM image of a 4-channel micro-ring resonator demultiplexer fabricated on a 220 nm top-silicon layer substrate (fabrication by BOOM partner AMO). The cross-section of the waveguides is 450×220 nm^2 and the micro-ring radius is as low as 17 um to obtain a large FSR per resonator. The transmission peaks of the micro-rings are spaced by 0.1 nm to achieve UDWDM operation.

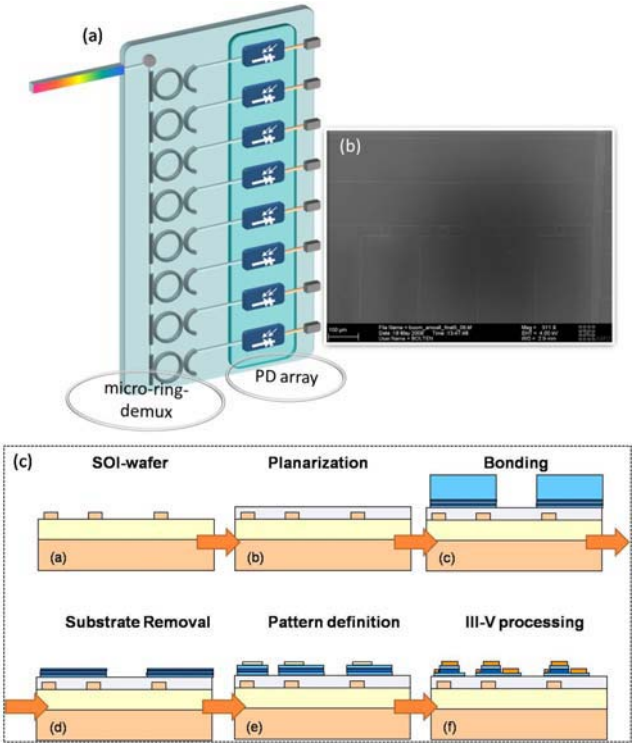

Figure 5: a) schematic view of UDWDM photodetector unit, b) 4-channel micro-ring resonator demultiplexer implemented in SOI nanowire technology and c) fabrication process

Figure 5c) illustrates the basic fabrication steps to be followed for the fabrication of the UDWDM photodetector. The process involves the bonding of unprocessed III-V dies on the SOI substrate and the removal of the III-V substrate through mechanical and chemical processing. Subsequently the photodetectors are fabricated through wafer-scale processing and are lithographically aligned to the underlying SOI waveguides (fabrication process implemented by BOOM partner IMEC).

2.4 Hybrid integrated silicon photonic transmitters

Figure 6 shows a schematic view of the EML transmitter module. The device incorporates two monolithic InP EML blocks flip-chip bonded on a 4um top silicon SOI substrate. Cascaded on-board SOAs are incorporated as on-chip amplifiers or shutters. The SOI board incorporates also the optical waveguides, a passive multiplexer, microstrip lines and electrical DC conductors and a SiGe BiCMOS driver to drive the modulators on-chip. The device is used to control the AOWC during the optical routing process and must exhibit fast rise and fall times.

Figure 6 shows a SEM view of a first generation EML device (device fabrication by BOOM partner HHI). The chip incorporates four different sections with different functionality: a) DFB laser, with five p-contact pads at the right side, b) SEP: passive waveguide to electrically isolate the laser from the modulator, c) MOD: modulator, with one p-contact pad at the left side, d) TAP: spot-size expander, as passive version without electrical contact. The etch pit and the long metallization stripe parallel to the waveguide on its left side, forming the surface n-contact common for all active sections, is also easily identified.

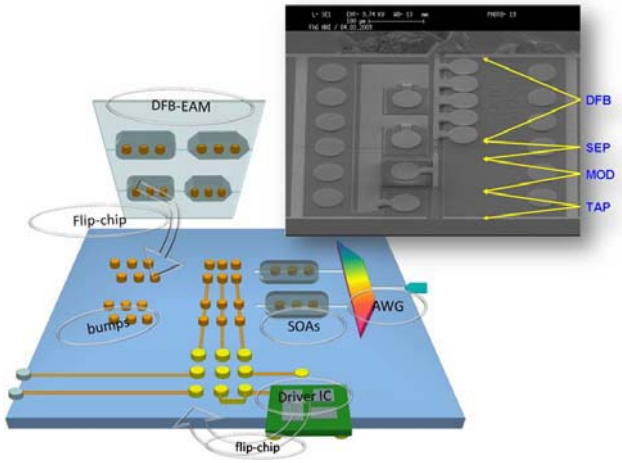

Figure 6: schematic view of EML transmitter unit and SEM image of monolithic InP flip-chip adapted EML

2.5 Micro-ring resonators for all-optical routing

BOOM also invests in the development of CMOS compatible waveguide technologies to fabricate ultra-small, waveguide structures. The project pursues two planar waveguide concepts: the TripleX^{TM} and SOI nanowire waveguide technologies. Based on these technologies BOOM aims to fabricate higher order micro-ring and racetrack resonators suitable for high-speed all-optical signal processing. In this section the micro-ring resonator

assisted all-optical wavelength conversion (RAWC) concept is presented. The RAWC employs a single SOA followed by a compact and integrated micro-ring resonator Reconfigurable Optical Add Drop Multiplexer (ROADM). The ROADM is fabricated using the TriPleX^{TM} waveguide technology (fabrication by BOOM partner LioniX B.V.) and features two coupled and tunable micro-ring resonators that provide a periodic spectral response with a filter pass-band profile suitable for high-speed chirp filtering.

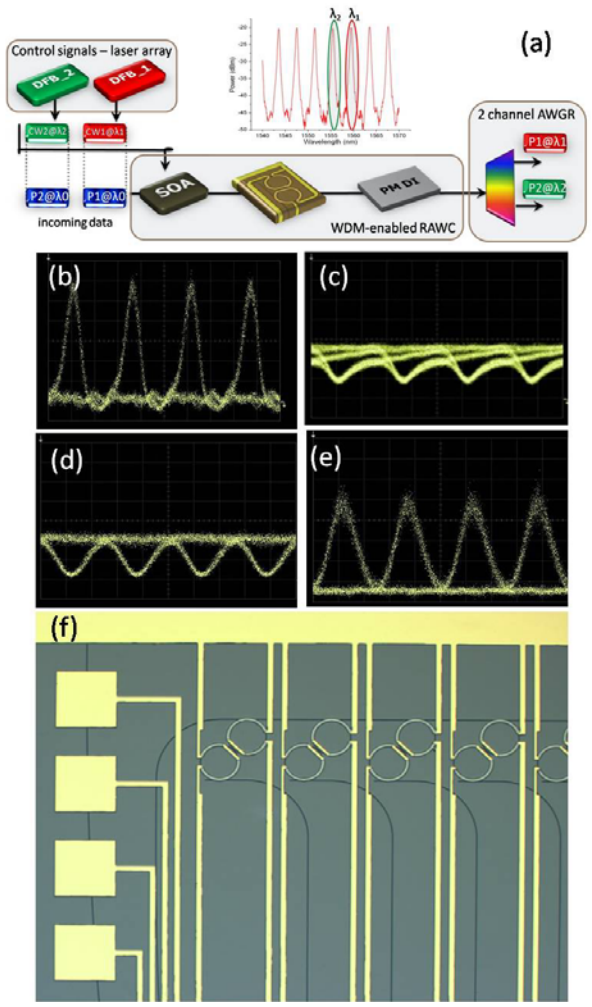

Figure 7: a) RAWC concept. Eye diagrams of : b) input signal, c) SOA output, d) ROADM output, e) DI output. f) SEM image of TripleX^{TM} ROADM

Figure 7a) shows the RAWC concept. Data packets enter serially the RAWC synchronized with CW packets generated by the router controller. The CW wavelengths are detuned with respect to the transmission peaks of the ROADM so chirp filtering for all the injected CWs is obtained. A delayed interferometer (DI) is used to restore the polarity of the pulses. Figures 7b) shows the eye diagram of the 40 Gb/s incoming data. Figure 7c) shows the inverted signal at the output of the SOA indicating the recovery of the amplifier beyond the 25 ps bit-slot. Figures 7d) and e) show the output of the ROADM and DI respectively, indicating the acceleration of the operational speed of the system as well as a clear eye opening for the converted signal at the output of the RAWC. Figure 7f) shows a fabricated array of ROADMs using the TripleX^{TM} technique indicating the potential of the RAWC concept for large scale photonic integration.

5. Conclusion

BOOM aims to develop compact, cost-effective and power efficient silicon photonic components to enable photonic Tb/s routers for current and new generation broadband core networks. The project is developing fabrication techniques as well as flip-chip bonding and heterogeneous III-V silicon integration methods to fabricate and mount the complete family of III-V components on SOI boards including: arrays of SOAs, EMLs and arrays of evanescent photodetectors. Here we have presented the basic device concepts and hybrid integration techniques that are currently being employed for the realization of the BOOM silicon routing concept.

6. Aknowledgment

This work is supported by the European Commission through project ICT-BOOM (www.ict-boom.eu) under the 7th Framework Programme (FP7), Information and Communications Technologies (ICT). Colleagues from HHI, IMEC, AMO GmbH, TUBerlin, TU/e, IHP, LioniX B.V. and TILAB are gratefully acknowledged for their contribution to this paper.

6. References

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7. Glossary

SOA-MZI:	Semiconductor-Optical-Amplifier based Mach-Zehnder Interferometer
AOWC:	All-optical wavelength converter
SOI:	Silicon-on-Insulator
EML:	Electro-absorption modulated laser
FSR:	Free spectral range
ROADM:	Reconfigurable Optical Add Drop Multiplexer