

Architecture, Design and Modeling of an Optically-Controlled Recirculating Buffer for 40 Gb/s Label-Switched Routers

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Abstract

We present a new scheme for all-optical contention detection and time-domain contention resolution of optical packets in label-switched routers that employ all-optical label recognition. The contention detection subsystem provides all the necessary control signals required to drive an optically-controlled buffer which employs 1x2 optical switching elements and an optical fiber delay line (FDL). The state of the buffer is dynamically controlled on a per packet basis with all the decisions and processing performed in the optical domain. Physical layer simulations show successful buffering and forwarding of 40 Gb/s optical packets with 2 dB power penalty.

I. INTRODUCTION

Recent advances in communications standards, such as the introduction of Multiprotocol Label Swapping (MPLS) and All-Optical Label Swapping (AOLS) have enabled the integration of the IP layer with the optical layer. In this context, research has been focused on identifying the functionalities required for AOLS and key technologies have been developed for their realization [1]. However, three major challenges have haunted the effort towards realizing true AOLS, posing specific requirements on both design and implementation; the lack of functional optical circuit designs, the lack of optical memory elements and the immaturity of photonic integration. Adapting to this reality, AOLS routers have been designed, shifting complex functionalities related to label processing, buffering and contention resolution to the electronic layer [2], [3].

The advances in photonic technology have verified that the realization of intelligent, all-optical control is not an elusive target. Initially, optical logic elements have been implemented using bulk components, whereas their integration with cutting-edge technology [4, 5] is now a reality. These elements have been used in devices resolving critical issues requiring intelligence and processing power, including buffering, scheduling and contention resolution. Very recent work has reported devices implementing all-optical recirculating buffers [6], wavelength-based contention resolution [7] and packet sorters [8]. This work has revealed the potential of the optical devices and has shown that optical signal processing can lead to unloading a number of functionalities from the electronic control layer directly to the optical domain. Going one

step further, the IST-LASAGNE project [9] aims at employing optical gates and flip-flops for building the first AOLS node. In this scenario, functionalities that have been handled by electronics such as label extraction and label processing are designed to be performed by optical gates. Optical flip-flops are used as latchable switches for routing purposes and wavelength-based switching fabrics have been designed for intra-node routing. Although promising, application-wise there is no design for contention detection, resolution and buffering based on all-optical signal processing, limiting the range of applications handled in the optical domain.

In this paper we present a new optical circuit design performing all-optical contention detection and resolution exploiting all-optical signal processing suitable for output-buffered AOLS nodes. All the decisions for forwarding or buffering of optical packets are made on-the-fly by a limited number of optical gates and memory elements. We validate the feasibility of the design through physical layer simulation using our developed model for a commercially available SOA-Mach-Zehnder interferometric gate (SOA-MZI).

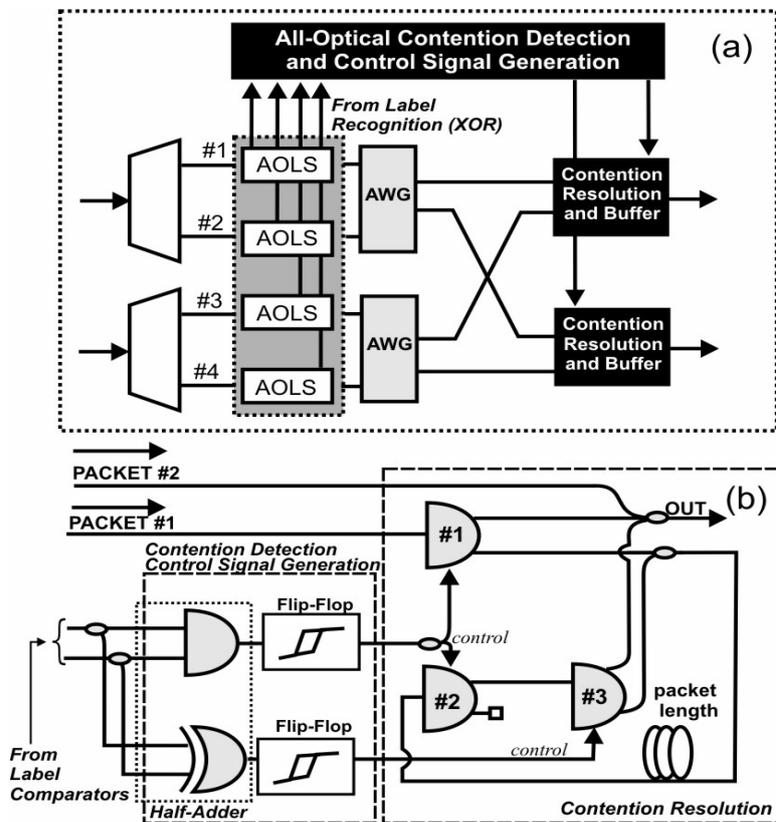


Fig. 1. (a) AOLS node architecture based on optical label processing and internal non-blocking wavelength routing and (b) logical design diagram of all-optical contention detection and resolution.

II. CONCEPT

A standard technique to forward optical packets in AOLS nodes (including the LASAGNE node) is via XOR correlation for label comparison. When a packet enters the AOLS node its label is optically extracted and compared with a number of locally generated labels. The result of this comparison determines on which wavelength and from which output port the packet will exit the node [Fig. 1(a)]. If the result of the label comparison is the same for two different optical packets, these packets will be

converted to the same wavelength and sent to the same output port leading to contention [9]. Figure 1 (a) shows the logical design of the sub-system. Contention is resolved in two stages; contention is firstly detected with simple all-optical Boolean logic and secondly, this logical result is used to control an all-optical recirculating buffer to sort out the contenting packets. The contention resolution block consists of a FDL and three optical gates configured to operate as 1x2 switches. Gate #1 is used to deflect the lowest priority packet inside the buffer; Gate #2 decides whether the buffer content should be discarded or not and Gate #3 decides whether a packet should exit the buffer or make another recirculation. Table 1 shows the truth table for the circuit. We assume that packet #2 has higher priority than packet #1, packet #3 is the content of the buffer and the buffer capacity is equal to one packet and. According to this table, when there is no contention and only one packet appears at the input of the contention resolution block (cases 3-6) the packet is directly forwarded to the output and the content of the buffer remains unchanged. If there are no packets present at the input (case2) the content of the buffer is forwarded to the output. In the case of contention (case 7 and 8) packet #2 is forwarded, the buffer is emptied and packet #1 enters the buffer.

TABLE I
Contention Resolution Truth Table

Case	P#1	P#2	P#3 Buffer	Pass	Buffer	Drop
1	0	0	0	-	-	-
2	0	0	1	P #3	0	0
3	0	1	0	P #2	0	0
4	0	1	1	P #2	P #3	0
5	1	0	0	P #1	0	0
6	1	0	1	P #1	P #3	0
7	1	1	0	P #2	P #1	0
8	1	1	1	P #2	P #1	P #3

To realize these functions the contention detection block should provide the appropriate control signals. More specifically, the contention detection block is an all-optical half-adder (HA) (fig. 2), which uses the XOR correlation result of the optical labels of packets 1 and 2 as inputs, whereas two optical flip-flops are used to provide packet-length control signals. Table 2 shows the corresponding truth table, realizing the following functions:

- Detection of an empty slot (case 1). Both outputs of the HA are '0' and all the 1x2 switches are operated in the bar state forwarding the buffer content to the output.
- Detection of one incoming packet (case 2 and 3). The buffer content is not altered and the incoming packet is forwarded from the input directly to the output. In both cases the XOR result of the HA is '1' and

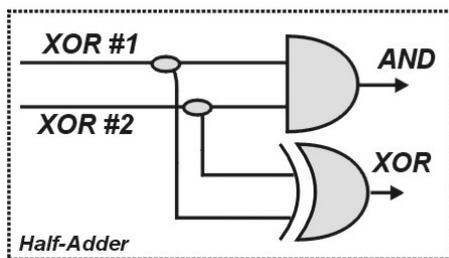


Fig. 2. Schematic diagram of half-adder circuit

TABLE II
Contention Detection Truth Table

Case	XOR #1	XOR #2	AND	XOR
1	0	0	0	0
2	0	1	0	1
3	1	0	0	1
4	1	1	1	0

configures gate #3 in the cross-state

forcing the buffer content to re-circulate.

- Detection of collision (case 4). In this case, gate #2 is operated in the cross state dropping the content of the buffer, packet #2 is forwarded to the output and packet #1 is buffered.

III. RESULTS AND DISCUSSION

The complete all-optical system was designed and simulated using a commercially-available simulation tool. In order to achieve high accuracy and good agreement with experimental results, the model chosen used a time-domain analysis of bi-directional optical fields within all active devices of the sub-system. We have designed the SOA-MZI model to closely match the experimental behavior of the 40 Gb/s 2R regenerator prototypes developed by Center for Integrated Photonics (C.I.P. UK) [10]. Fig. 3 shows the comparative study between experimental and simulated results. Fig. 3(a) and (b) show static gain measurements of the SOAs used within the optical gates, showing good agreement. Additionally, Fig. 3(c) and (d) show pump-probe measurements for characterizing the gain recovery time of the SOAs. The inset shows eye diagrams for 10 Gb/s wavelength conversion obtained experimentally and from simulation. The response time was measured 25 ps and 23 ps at 1/e point, experimentally and using the simulation model respectively. Finally, the extinction ratio of the 1x2 optical switches was 15 dB.

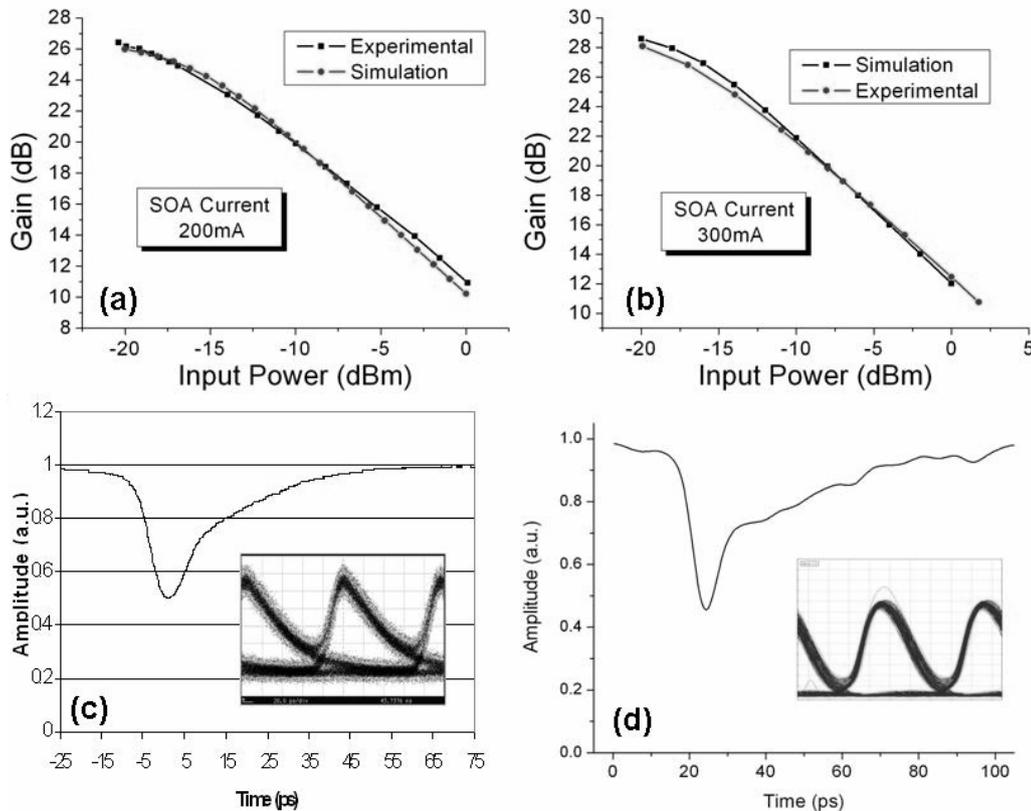


Fig. 3. Comparison between simulation and experimental results. SOA gain response when operated at (a) 200 mA and (b) 300 mA. Recovery time measurements (c) provided by supplier and (d) using the simulation model. Insets show corresponding 10 Gb/s wavelength conversion.

Two scenarios were simulated to demonstrate the functionality of the circuit at 40 Gb/s.

Fig. 4 shows the time-domain results for scenario A (left column) and scenario B (right column). For both cases rows a) and b) show the packet streams entering the contention resolution block, row c) shows the content of the buffer and row d) shows the common output of the system. In case A packets P1 and P3 enter simultaneously the contention resolution block with P1 being the highest priority packet. The logical AND result of the HA forces gate #1 to operate in the cross state deflecting P3 inside the buffer whereas P1 appears at the output of the circuit. In the next time instance packet P2 appears at one input of the circuit. The AND result of the HA is now '0' and gate #2 is operated in the bar state forwarding P3 to gate #3. The XOR result of the HA being a logical '1' forces gate #3 to operate in the cross state leading to a re-circulation for P3 in the FDL so that P2 can be forwarded to the output without any collision. In the next time instance an empty time slot is detected and all three gates of the buffer are operated in the bar state so that P3 'fills' the empty slot and appears at the output. Similarly, in scenario B the contention between P1 and P4 leads to the buffering of P4 in the FDL. P4 is then forced to re-circulate as one packet (P2) is detected at one input of the circuit. In the next time instance two packets appear at both inputs of the circuit. It is the only case where the AND result of the HA is '1' and gate #2 is operated in the cross state dropping P4, as we have assumed a packet length FDL. Then P5 enters the buffer, P3 is forwarded to the output and when an empty slot is detected, P5 appears at the output.

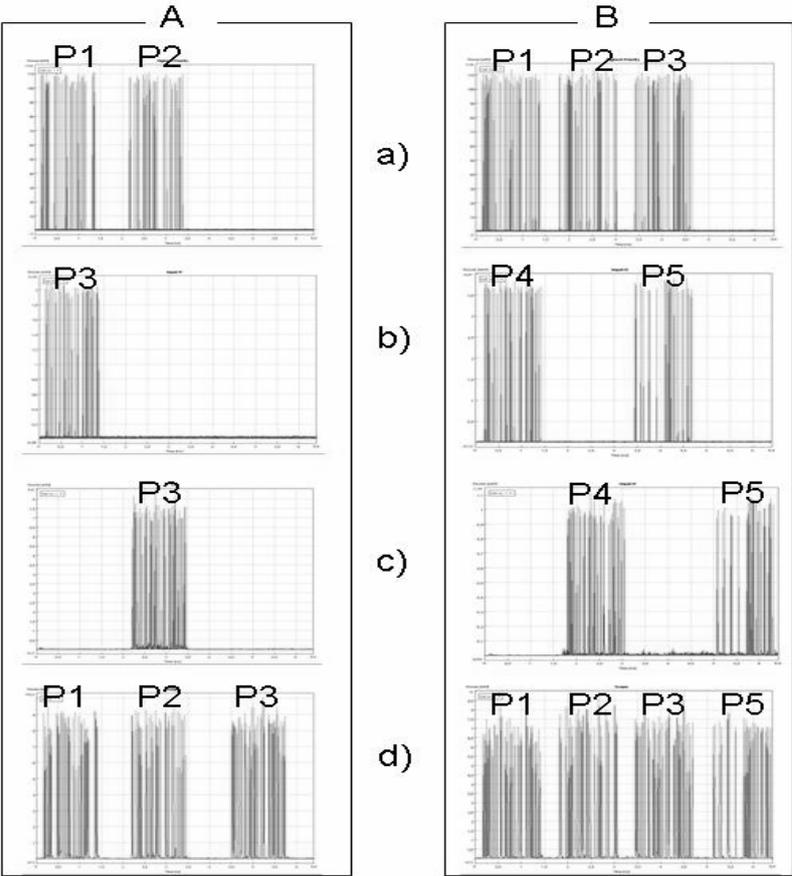


Fig. 4. Time-domain traces for simulated scenario A (left column) and B (right column). Row a) high priority incoming packets, b) low priority incoming packets, c) buffer content and d) output of the system.

Fig. 5 shows BER measurements carried out in order to investigate the penalty induced

due to packet propagation through the optical buffer. The results show that receiver power penalty of 3 dB was obtained at the output of the system, which was reduced to 2 dB through 2R regeneration at the output.

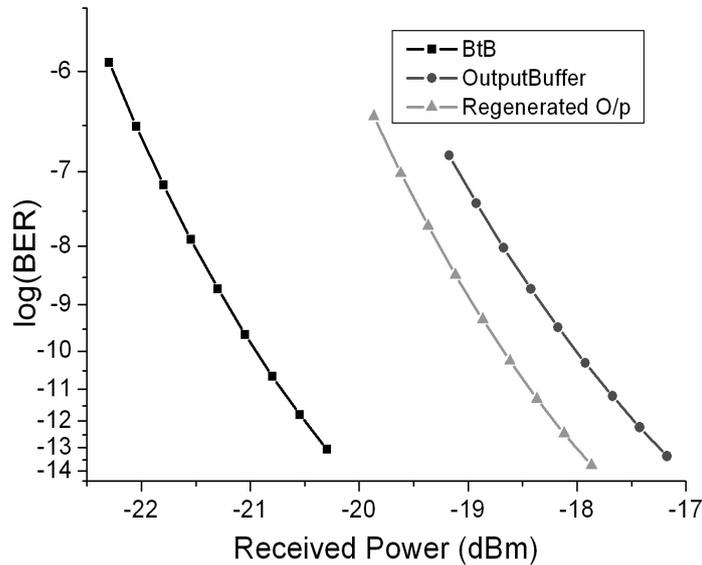


Fig. 5. Bit Error Rate measurements for back-to-back and output of the system before and after 2R regeneration

IV. CONCLUSION

We presented a new design for all-optical contention detection and contention resolution for all-optical nodes that use optical gates for intelligent processing. The combination of the contention detection and contention resolution block provides a buffering system that is configured on a per packet basis sorting out contenting packets. The system requires only the result of the label comparison to operate, which means that no extra overhead in the labels or control signaling for contention resolution is required.

Acknowledgements

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