ALL-OPTICAL PACKET CLOCK RECOVERY CIRCUIT

K. Yiannopoulos (1), N. Pleros (1), C. Bintjas (1), M. Kalyvas (1), G. Theophilopoulos (1), H. Avramopoulos (1) and G. Guekos (2)
1: Department of Electrical and Computer Engineering, National Technical University of Athens, Zographou, GR 15773, Athens, Greece
E-mail: kyianno@cc.ece.ntua.gr
2: Swiss Federal Institute of Technology Zurich, ETH Hoenggerberg, CH-8093 Zurich, Switzerland

Abstract *We present an all-optical clock recovery circuit for data packets at 10 Gbps. The circuit uses a Fabry-Perot filter and a UNI gate and acquires clock within a few bits.*

Introduction

A suitable concept to take advantage of the capacity afforded by optical networks is optical packet switching. Key elements to achieve optical packet switching are both high level functions like header extraction and processing and lower level ones such as optical gating and bit manipulation [1]. A very important issue when dealing with all-optical signal processing is powering and synchronizing the optical gates and subsystems that form the whole circuit [2]. This issue can be addressed with the introduction of a control signal that will power and synchronize the optical gates, whenever optical packets are present in the circuit. For this to become possible, a unit capable of providing a clock signal only for the duration of the packet is necessary. So far, clock recovery has been illustrated using synchronized mode-locked ring lasers [3], electrical phase-locked loops [4], self-pulsating DFB lasers [5] and Fabry-Perot filters [6]. These techniques have provided impressive results but are not particularly suitable for very short packets because they do not have immediate locking times.

In this paper we demonstrate a novel technique for recovering the clock out of data packets. It uses a Fabry-Perot filter to pre-filter the incoming data packet and generate partial '1s' in the space of '0s' and a high speed, non-linear, optical gate to equalize the partial '1s'. With this technique we show that it is possible to generate a clock signal which is approximately equal to the original packet length with locking time of only a few bits long. This circuit is self-synchronising, has no high speed electronics and is apppropriate for all-optical signal processing in optical, packet switched network architectures.

Concept and Experimental Setup

One very interesting feature of Fabry-Perot filters is their exponentially decaying time-domain impulse response, the lifetime of which is determined by the filter finesse. As a result of this, if a random bit sequence at a line rate equal to the filter free spectral range is fed into it, the '0' bit sequences will be partially filled by preceding '1s'. However, the Fabry-Perot filter cannot be used as a stand-alone clock recovery element, since it will provide a highly amplitude modulated output from our random input bit stream. The amplitude modulation at the output of the Fabry-Perot may be reduced by taking advantage of the non-linear switching function of a high speed, optical gate like the SLALOM or the UNI [7-12].

The experimental setup is shown in Figure 1. The pseudo data pattern is produced using a gain-switched DFB laser diode operating at 1549.2 nm, which provides 8 ps pulses at 1.29075 GHz, after linear compression through DCF fiber. The output of the diode is modulated into the 2^7-1 PRBS, using a $LiNbO_3$ modulator (MOD1) and a PRBS pattern generator. The PRBS is then 3-times bit interleaved and multiplexed thus producing a pseudo-data pattern at 10.326 GHz. A second modulator (MOD2) driven by a pulse generator is employed in order to produce variable length data packets.

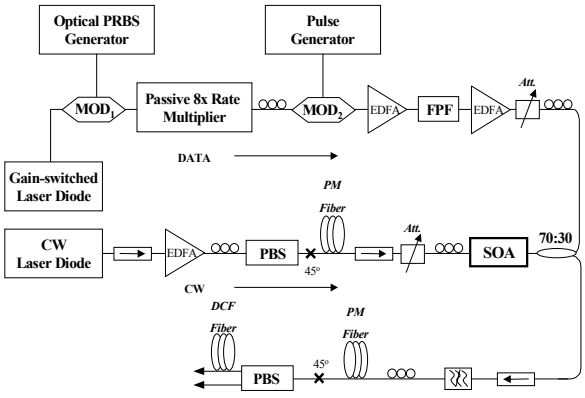

Figure 1 Experimental setup

The data packets are then fed into the Fabry-Perot filter with FSR equal to the line rate and finesse equal to 20.7. The output of the Fabry-Perot filter is used as the control signal, which drives the UNI gate. A second DFB operating at 1545 nm provides the second CW signal, which is switched by the control signal. The two signals travel in opposite directions through the gate and the control signal information is imprinted on the CW signal through the

non-linear response of the gate. The active element of the UNI gate is a commercially available 1.5mm bulk InGaAsP/InP ridge waveguide SOA with 27 dB small signal gain at 1550 nm, 24 dB at 1545 nm, 3 dB polarization gain dependence and a recovery time of 100 ps for 700 mA of drive current.

Before entering the SOA the CW signal is split into two components, which are time-delayed by 50 ps, using 25 m of PM fibre. The gate is arranged so that the control signal accesses only one of the two orthogonally polarized CW components. At the output of the gate the two CW components have their differential time delay removed and are made to interfere on a PBS. By arranging for the differential phase between the two components to be nearly π, a sequence of consecutive '1s' appears at the output of the gate.

Results and Discussion

Typical results are shown in Figure 2. Packets of different contents where used to verify the operation of the clock recovery module. The packets are 3 ns long, time duration which is translated into 30 bits, and have period of 6.2 ns. Figures 2 (a) and (b) show the initial contents of the packets. Figures 2 (c) and (d) display the corresponding outputs from the Fabry-Perot filter showing a 10 GHz signal with a strong pattern modulation and figures 2 (e) and (f) show the recovered clock at the output of the UNI gate.

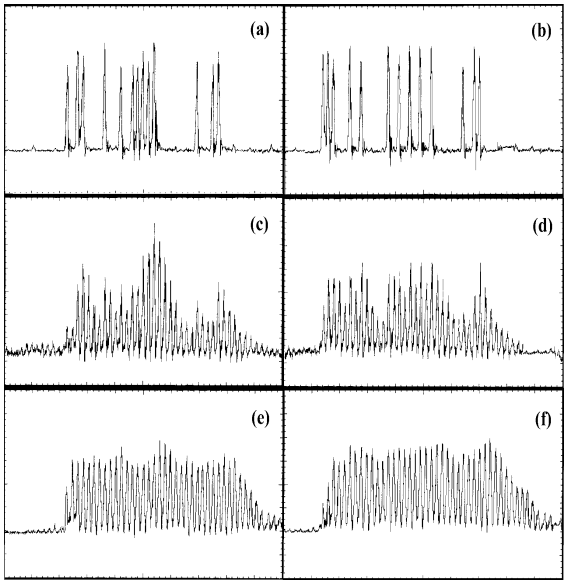

Figure 2 (a), (b) Two different data packets, (c), (d) Corresponding outputs from the FP filter (e), (f) Output of the UNI gate for both packets. The time base is 500 ps/div

The recovered clock signal locks to the incoming data packet within a few bits and persists for the length of the packet extended only by the lifetime of the Fabry-Perot filter. The rise time of the clock signal is reduced after transit through the UNI gate. This is because the gain of the SOA is less saturated at the front end of the packet and results in a sharper leading edge. The locking time of the circuit depends on the finesse of the Fabry-Perot filter and for the different data pattern examples tried it was always less than 3 bits long. The choice of the finesse of the filter must be made as a compromise between having a circuit with a fast capture time and a circuit that provides a clock signal of low amplitude modulation for a given sequence of consecutive '0s'. The amplitude modulation (highest to lowest pulse ratio) of the recovered clock signal was measured and was found to be less than 1.5 dB in all cases for the 30 bits corresponding to the original packet. Switching power and mean energy per pulse for the CW and the control signal were 155 μW and 30 fJ, respectively.

The circuit was also numerically modelled to investigate how to choose the finesse of the Fabry-Perot. It was found that for filters with finesse higher than 20 and packets with 6 consecutive '0s' as in the present experiment, the rise time of the clock signal was always less than 3 bits and the amplitude modulation was less than 1.5 dB. Correspondingly simulations for data patterns with 30 consecutive '0s' and a filter with finesse 80, have shown that the circuit produces clock signal that is modulated by less than 1.5 dB.

Conclusions

We have presented a novel clock recovery module, which can be used for powering and synchronising optical subsystems for packet switched optical networks. The circuit has no high-speed electronic components, does not require synchronisation and acquires locking within a few bits.

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