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ALL- OPTICAL CLOCK RECOVERY FOR DATA PACKETS

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Abstract : *An all-optical clock recovery unit is demonstrated at 10 Gbps, appropriate for use with short optical packets. The circuit uses a Fabry-Perot and a UNI gate and achieves clock recovery within a few bits.*

Introduction

The growing Internet bandwidth demand and the advent of new diverse telecommunications services brought about the need for transparent, intelligent optical networks. A key function for implementing networks like these is packet or bit synchronization, achieved by clock recovery systems [1,2]. So far, clock recovery has been obtained using a variety of techniques including synchronized mode-locked ring lasers [3], electrical phase-locked loops [4], self-pulsating DFB lasers [5] and Fabry Perot filters [6]. These techniques have provided very impressive results but are not particularly suitable for packets because they do not have immediate capture times.

One very interesting feature of a Fabry Perot (FP) etalon is that its impulse response function in time, is a decaying exponential function whose lifetime is determined by the filter finesse. This means that if an RZ modulated data signal is introduced in a FP filter with a free spectral range equal (FSR) to the line rate, the '0s' at the output of the filter will be partially filled by preceeding '1s'. Furthermore given that the FP is a passive device, its locking time will be only a few bits long and again determined by its finesse. Despite these properties a FP etalon cannot be used on its own for clock recovery, because the output clock will be highly modulated depending on the input data pattern. This shortcoming of the FP maybe mitigated using a high speed optical nonlinear gate at the output of the filter. Optical nonlinear gates [7,8] like the UNI have been used in a number of applications [9-11] and have demonstrated their high speed potential.

Therefore in this letter we describe a novel technique for recovering the clock out of data packets, using a FP to pre-filter the data sequence followed by a UNI gate to equalize the amplitude of the '1s'. With this technique we show that it is possible to generate a clock signal approximately equal to the original packet length and the locking time is only a few bits long. The proposed clock recovery circuits has no high speed electronics and is apppropriate for all-optical header processing and routing functions in packet switched network architectures.

Experiment

The experimental setup is shown in Figure 1. A gain switched DFB laser operating at 1549.2 nm provides 8 ps pulses at a 1.29075 GHz, after linear compression through DCF fiber. The output of the laser is modulated with a 2^7-1 PRBS, using a $LiNbO_3$ modulator (MOD1) and a PRBS pattern generator and is 8 times time-interleaved to generate a 10.326 GHz bit stream. The variable length data packets are produced using a second modulator (MOD2) and a pulse generator.

The pseudo data packets are next introduced in a FP filter with FSR equal to the line rate and a finesse of 20.7. The output of the FP filter is then used as the control signal in a UNI gate optimized for operation a at 10 GHz. The second signal into the UNI gate is CW and is provided by a DFB at 1545 nm. The UNI is arranged to function as a counter-propagating Boolean AND gate, and the control signal is written on the CW signal through the nonlinear transfer function of the gate. The UNI uses a commercially available 1.5mm bulk InGaAsP/InP ridge waveguide SOA with 27 dB small signal gain at 1550 nm, 24 dB at 1545 nm, 3 dB polarization gain dependence and a recovery time of 100 ps, when driven with 700 mA dc current.

With this arrangement the control pulses from the FP filter are adjusted to be co-polarized with one of the two relatively delayed, polarization components of the CW signal and imprint themselves on the phase of this CW component. The delay between the two CW

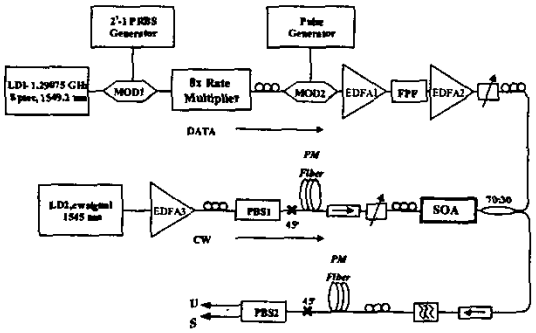

Figure 1 Experimental Setup

polarization components is then removed in the same length of PM fiber, and these are recombined on PBS2. The power of the control signal is arranged so that the differential phase shift between the two polarization components in the SOA is close to π, resulting in a sequence of nearly equal amplitude '1s' at the output of the gate.

Results

Packets of different contents were tested to prove the functionality of the system and figure 2 shows representative results from the circuit. Figures 2 (a) and (b) show the original contents of the packets. The packets are 3 ns long, contain 30 bits and have period of 6.2 ns. Figures 2 (c) and (d) display the corresponding outputs from the FP filter showing a 10 GHz signal with a strong pattern modulation and figures 2 (e) and (f) show the recovered clock at the output of the UNI gate.

Switching power and mean energy per pulse for the CW and the control signal were 155 μW and 30 fJ, respectively. In these examples the amplitude modulation (highest to lowest pulse ratio) on the 30 bits corresponding to the original packet is less than 1.5 dB. Rise time reduction is obtained as well. It is evident that clock recovery is obtained at the first few (2) bits of the packet. Therefore only minimal guardband is required between the packets, compared to other clock recovery methods. Due to the FP lifetime, the trailing edge of the packet clock decays more slowly and is of the order of 7 bits. Clearly using a FP with a higher finesse will assist to reduce the amplitude modulation of the packet clock, at the expense of a slower rising and fall time of the packet. However it should be noted that these rise and fall times are defined by the finesse of the FP as fixed numbers of bits and are independent of the rate. Therefore given that the UNI gate may operate at higher data rates, by choosing a FP of the appropriate FSR, this clock recovery circuit should operate and the guardband required will scale with the bit period.

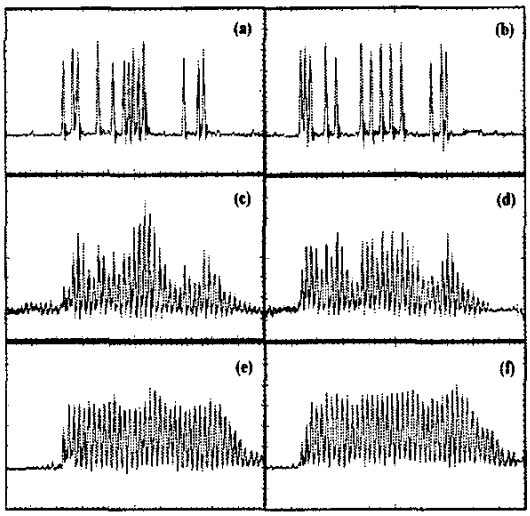

Figure 2: (a), (b) Two different data packets, (c), (d) Corresponding outputs from the FP filter (e), (f) Output of the UNI gate for both packets. The time base is 500 ps/div.

The system was also tested using a non-packeted (MOD2 was kept transparent) pseudo-data signal and the amplitude pattern imposed on the extracted clock was found to be less than 1.2 dB. The extracted clock was also monitored on a 50 GHz RF Spectrum Analyzer, both for packet and for full pseudo data signals. The derived clock signal displayed suppression of the data modes in excess of 40 dB compared to the clock component and the rms timing jitter was found to be less than 5 ps. It should be noted that the timing jitter of the incoming data signal was of the same order due to the x8 bit interleaver.

Conclusions

In conclusion we have presented a novel clock recovery scheme, which can be used for data packet networks. The circuit has no high-speed electronic components, does not require synchronisation and acquires locking within a few bits. Given that the UNI gate has been shown to operate in excess of 100 Gbps, it should be possible to operate at these rates and without impairment to the length of the guardband between packets that it requires.

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