10 Gb/s Transmission and Thermo-Optic Resonance Tuning in Silicon-Plasmonic Waveguide Platform

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Abstract: The first system-level experimental results of hybrid Si-DLSPP structures incorporated into a SOI chip are reported. We demonstrate over 7nm thermo-optical tuning of a Si-Plasmonic racetrack-resonator and verify error-free 10Gb/s transmission through 60um Si-Plasmonic waveguide.
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1. Introduction

It is no secret that the requirements in integration density and power consumption of high-capacity inter-connects are already exceeding their practical limits, rising massive questions about next generation deployments [1]. To this end, the exploitation of plasmonic technology in short distance, chip-to-chip and on-chip transmission applications, has recently attracted the attention of the photonic community mainly due to the reduced footprint, power consumption and enhanced light-matter interaction attributes that plasmonic waveguiding has to offer [2]. Furthermore, as silicon photonics evolve to a powerful technology for low-cost integrated optical connectivity [3], the incorporation of silicon and plasmonic devices on the same technology platform emerges as the forthcoming challenge in photonics data transmission systems [4].

Up to now, a limited number of articles have been presented reporting design and fabrication achievements of plasmonic waveguides on Silicon–on–Insulator (SOI) platforms. Recently 80% coupling efficiency between silicon and plasmonic propagation has been demonstrated for Conductor-Gap-Silicon (CGS) plasmonic waveguides [5] as well as for Dielectric Loaded Surface Plasmon Polariton (DLSPP) waveguides [6]. Moreover, the static operation of a hybrid Si-Plasmonic ring resonator [6] and the thermo-optic functionality of a plasmonic Mach-Zehnder Interferometer (MZI) integrated on Magnesium Fluoride (MgF2) substrate [7] have been reported. However, the next step to the evolution of plasmonic technology requires the mutation of proof-of-concept demonstrations to performance evaluations of operational Silicon-Plasmonic structures, in actual datacom applications.

In this article, we present for the first time, to the best of our knowledge, a hybrid Si–Plasmonic chip that incorporates more than one hundred single plasmonic devices integrated on a SOI platform. Less than 3dB Si-to-DLSPP coupling is reported, while adequate thermo-optic operation of the devices is verified by successfully tuning the resonance of a plasmonic ring resonator over a 7nm wavelength range, enhancing the potential of the hybrid Si-

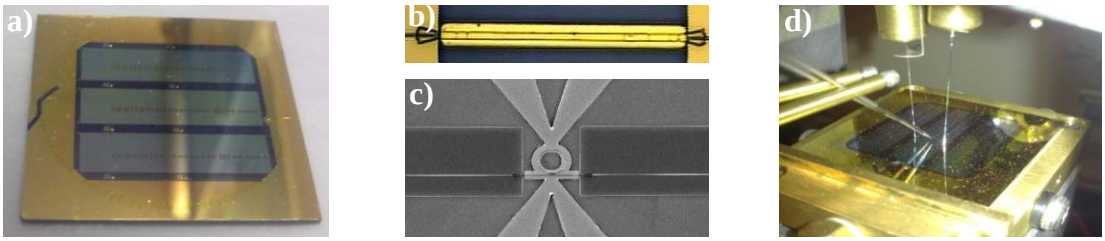

Figure 1: (a) The hybrid Si - Plasmonic chip, (b) Straight DLSPP waveguide of 60um, (c) All – Pass Racetrack Ring Resonator, (d) Chip on Probe Station

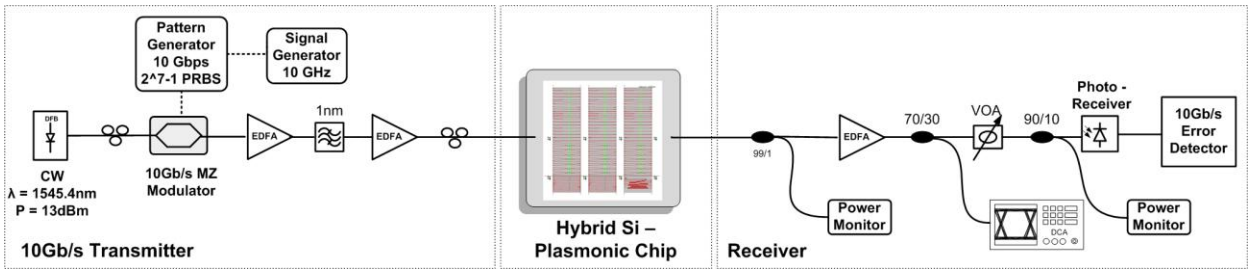

Figure 2: Experimental Setup of the 10Gb/s transmission experiment through the straight DLSPP waveguide

Plasmonic integration concept. Finally, we demonstrate the first reported data transmission in Silicon-Plasmonic technology with the transmission of a 10Gb/s Non–Return–to–Zero (NRZ) signal through a 60um long Si–Plasmonic waveguide. The achieved error-free operation and the negligible (<0.2dB) power penalty denote the remarkable transmission performance of the Si–Plasmonic structures.

2. Experimental Setup

Figure 1(a) illustrates the Silicon-Plasmonic chip carrying more than one hundred Silicon-Plasmonics structures such as single waveguides, various ring resonator types and Mach-Zehnder (MZ) switches. The chip comprises three Silicon-on-Insulator motherboards, properly configured to enable the hybrid integration of plasmonics. The hosting areas of the plasmonic structures on each motherboard have been etched forming 200nm-deep cavities in the Silicon Dioxide substrate. The cavities were covered with 65nm-thick and 3um wide gold film, on top of which a strip of Polymethylmethacrylate (PMMA) dielectric material with a cross-section of $600x500nm^2$ was placed, forming Dielectric Loaded Surface Plasmon Polariton (DLSPP) waveguide configuration on silicon dioxide substrate. Figure 1(b) shows a 60um long straight waveguide based on the previously mentioned configuration. Since Surface Plasmon Polaritons (SPP) support only TM propagating mode, the SOI motherboard was equipped with TM grating couplers and employed $340x400nm^2$ silicon rib waveguides with 50nm-thick slab, which exhibit adequate characteristics for TM propagation. Additionally, the integration of plasmonics in the silicon chip was based on a butt-coupling approach that was adopted for interfacing the Silicon to the DLSPP waveguides. Figure 1(c) shows a plasmonic racetrack ring resonator with 5.5um radius of curvature, 0.35um gap and 0.8um interaction length, followed by 20um straight DLSPP waveguides. The gold layer of the device was connected to gold pads enabling current injection in the chip. The functionality of the chip's structures was evaluated both in terms of data transmission performance as well as of thermo-optic operation.

The thermo-optic performance of the plasmonic structures was evaluated through the characterization of an all–pass racetrack ring resonator, identical to the one depicted in Figure 1(c). A continuous wave (CW) signal was generated by a tunable laser with a tuning range of 1500 to 1580nm and step resolution of 10pm. This signal was then used as input to the plasmonic ring resonator that exhibited 12dB losses at 1545nm.TM-polarization state of the incoming light was ensured with a polarization controller before entry into the hybrid Silicon–Plasmonic ring. Current injection was enabled by utilizing electrical tips placed on the pads of the device. Step-by-step measurements of the output power were taken by scanning through the full range of the tunable laser initially without employing current, for reference purposes, and later for 50mA current. The respective spectral responses were reconstructed by plotting the values of the output power versus the wavelength steps.

Following this, the transmission performance of the plasmonic waveguides was assessed in a 10Gb/s transmission experiment. The experimental setup that was used for the evaluation process is depicted in Figure 2. A CW signal at 1545.4nm was launched into a $Ti:LiNbO_3$ MZ modulator driven by a Pseudo-Random-Bit-Sequence (PRBS) pattern generator, yielding a 10Gb/s 2^7-1 NRZ data sequence at its output. The signal was then amplified by an Erbium-Doped-Fiber-Amplifier (EDFA) chain, providing 24dBm output, and launched into the plasmonic waveguide. The losses of the waveguide were found to be 11dB at 1545nm for TM-polarized light, and can be analyzed, based on cutback measurements on 60, 80 and 100um long DLSPP samples, to 6dB propagation losses and 2.5 dB coupling losses per Si-to-DLSPP interface. The data signal at the output of the plasmonic waveguide was amplified and fed into a high–sensitivity Photo-Receiver connected to a 10Gb/s Error Detector in order for Bit Error Rate (BER) measurements to be performed.

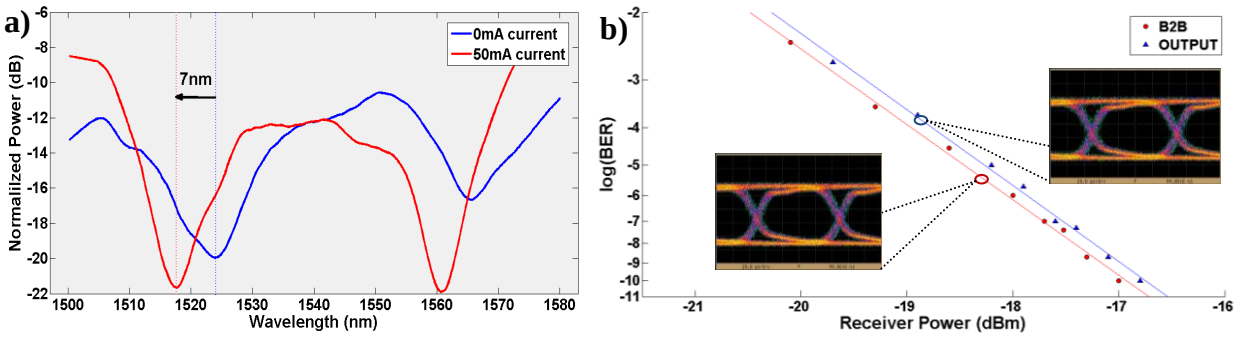

Figure 3: (a) Spectral Response of racetrack ring resonator over the range of 1500 - 1580nm, (b) BER measurements and Eye Diagrams of the B2B and the transmitted, though the 60um Si-DLSPP waveguide, signal

3. Results and Discussion

Figure 3(a) shows the characterization results of the thermo-optic tuning of the racetrack ring resonator in the range of 1500 to 1580nm for two current injection states. The blue line represents the spectral response of the device for 0mA injected current (COOL state) while the red line corresponds to the spectral response that is obtained for 50mA injected current (HOT state). The simultaneous shifting of the two resonances suggests thermo-optic tuning of the device by 7nm towards smaller wavelengths, owing to the negative sign of the thermo-optic coefficient of PMMA [7]. Returning, however, to the initial state of the ring resonator, after switching off current, was not achieved, implying that the reversibility of the device was lost, most probably due to heating it above the maximum service temperature of the PMMA strip [7]. It becomes clear though that better results could be expected with the use of a material that will be more tolerant to high temperature operation.

Figure 3(b) shows the BER curves obtained for the 10Gb/s data transmission through the straight DLSPP waveguide. Error–Free operation was obtained for the transmitted signal with a power penalty of less than 0.2dB against the B2B measurements, implying no impact on the transmitted signal as confirmed by the eye diagrams at the inset .

4. Conclusion

We have presented the first system-level experimental results of hybrid Si-DLSPP structures incorporated into a SOI chip. The thermo-optic performance of the proposed configurations was identified through the wavelength tuning of a plasmonic ring resonator over more than 7 nm while error–free operation with negligible power penalty (<0.2dB) was obtained for a 10Gb/s NRZ signal transmission through a 60um straight plasmonic waveguide. The reported results denote the strong potential of the Si-Plasmonic integration concept towards the penetration of plasmonic technology in actual datacom applications.

5. Acknowledgment

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