CLOCK AND DATA RECOVERY WITH SOA-BASED OPTICAL GATES

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Abstract *We present optical clock and data recovery for 10 Gb/s asynchronous packets. The original data are sampled with an optical gate powered by clock packet, generated with a novel packet clock recovery circuit.*

Introduction and concept

Optical packet switching techniques promise to help photonic networking by increasing bandwidth efficiency, providing greater capacity and overcoming limitations imposed by electronic processing at intermediate routing nodes and endpoints [1]. In such networks, the asynchronous origin of the traffic flow requires special characteristics for network elements, such as clock and data recovery (CDR) circuits. The ability to generate independent packet clock signals and to process on a packet-by-packet basis at the bit -level, is of key importance for such elements. Typical CDR circuits consist of a clock recovery unit and a decision element and several techniques have been proposed for this purpose. The majority of them employ electronic circuitry and operate with low-rate data traffic [2,3], whereas 10 Gb/s CDR configurations require long synchronization preamble signals [4]. Optical clock recovery circuits capable to handle asynchronous traffic have been shown [5-7], but no optical CDR circuits have yet been reported.

In this presentation we demonstrate for the first time to our knowledge, an all-optical CDR circuit for short, asynchronous 10 Gb/s data packets. The circuit consists of a packet clock recovery unit [5], capable of extracting the local clock within only a few bits, followed by an Ultrafast Nonlinear Interferometer (UNI) gate, used as the optical decision element. The packet clock recovery circuit comprises of a Fabry-Perot (FP) filter used as a passive oscillator and a UNI gate acting as a hard limiter to smooth out the amplitude modulation induced by the FP filter. A second UNI gate performs data recovery by ANDing each original data packet with its corresponding packet clock and regenerates the recovered signal. The circuit is self-synhronizing, has low locking time, requires short guard-bands between successive packets, requires no high-speed electronics and may be ideally used for all-optical processing of asynchronous packets.

Experiment

Fig. 1 depicts the experimental setup consisting of an asynchronous packet flow generator, the clock recovery circuit and an all-optical AND gate. The

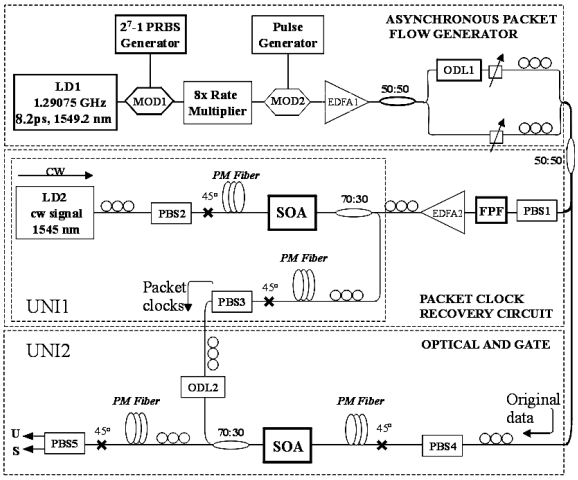

Figure 1: Experimental Setup.

optical signal was generated with a DFB laser (LD1) at 1549.4 nm, gain switched at 1.29075 GHz and providing 8.2 ps pulses. This pulse train was modulated with a 2^7-1 PRBS pattern in a Li:NbO_3 modulator (MOD1) and was 3-times bit interleaved to form a pseudo-data pattern at 10.326 Gb/s. Synchronous data packets were produced using a second modulator (MOD2) driven by a programmable pulse generator. These were time-multiplexed in a fiber split-and-combine packet flow generator designed to induce 30.6 ns relative delay between its two arms. Fine phase adjustment of successive packets to study asynchronous operation, was achieved using a variable optical delay line (ODL1) placed on one path of the flow generator.

The asynchronous packets were then inserted in the subsystems of the CDR circuit. The clock recovery unit consisted of a FP filter with free spectral range equal to the line rate and a finesse of 20.7, and a UNI gate (UNI1) [5]. Introduction of each data packet into the FP filter leads to partial filling of the '0's in the data stream due to the lifetime of the filter, forming a packet clock resembling signal with intense amplitude modulation. This was used as the control signal in a UNI gate powered by a counter-propagating CW signal from DFB laser LD2 at 1545 nm. This arrangement forces amplitude equalization through the nonlinear transfer function of the gate and results in a packet clock of similar length to the original

packet [5]. The active nonlinear element of UNI1 was a 1.5 mm bulk InGaAsP/InP ridge waveguide SOA with 27 dB small signal gain at 1550 nm, 24 dB at 1545 nm and a recovery time of 80 ps, when driven with 700 mA dc current. Sampling of the data packets occured in a second UNI gate (UNI2) built identically to UNI1, by ANDing the incoming data packets with their corresponding self-extracted packet clocks. Optical delay line (ODL2) was used at the output of UNI1, to synchronize statically the data packets with their equivalent clock and to ensure good switching at the S-port of UNI2.

Results

Data packets of adjustable length, period and content, were used to test the performance of the system at 10 Gb/s nominal rate. Fig. 2(a) indicates a sequence of 4 asynchronous packets each consisting of 41 bits (~4 ns duration). Packets #1 and #3 are phase misaligned with packets #2 and #4, with time intervals as depicted in Fig. 2(a). Fig. 2(b) shows the equivalent recovered packet clocks, while Fig. 2(c) illustrates the packet stream at the S-port of UNI2. Successfull operation of UNI1 was achieved for 0.9 mW of CW optical power and 100 fJ of control pulse energy. The pulse energies for the packet flow and the recovered clock signals interacting in UNI2 were 2 fJ and 22 fJ, respectively. The eye and pulse traces shown in Fig. 3 provide information on the regenerative properties of the circuit. Fig. 3(a) shows packet #4 and fig. 3(b), shows the eye diagram of the asynchronous data stream for phase adjustment typical of asynchronous packet arrival. The amplitude and timing jitter as they appear on the original signal are due to imperfect rate multiplication and packet generation. Fig. 3(c), (d)

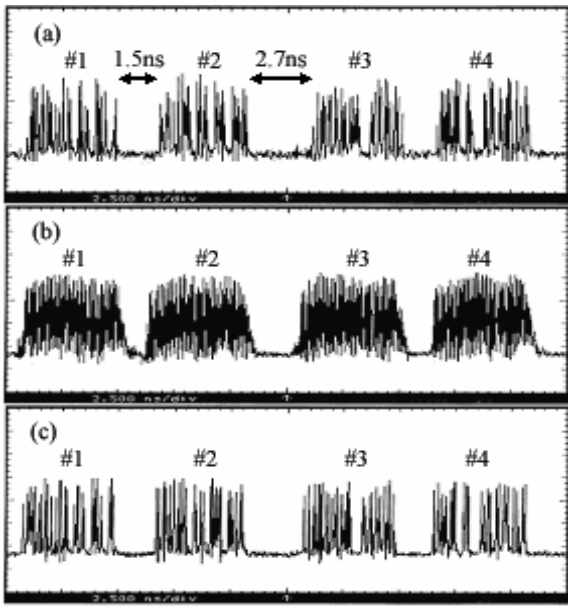

Figure 2: (a) Incoming asynchronous data packets, (b) Recovered packet clocks at exit of UNI1, and (c) Recovered data packets at exit of UNI2.

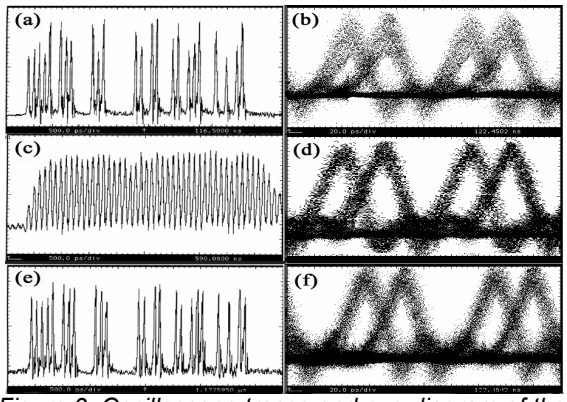

Figure 3: Oscilloscope traces and eye diagram of the: (a), (b) original asynchronous packets, (c), (d) recovered clock packets, and (e), (f) recovered data. The time base of pulse and eye traces is 500 ps/div and 20 ps/div, respectively.

show the good quality extracted packet clocks with rise and fall times of 2 and 8 bits respectively. Fig. 3(e),(f) illustrate the corresponding S-port output of UNI2 and confirm the improvement of the recovered data in terms of amplitude modulation and timing jitter. Measurements were also carried to investigate timing jitter performance, using microwave spectrum analysis for better accuracy. The measured timing jitter was 1.5 ps for the original data, 300 fs for the recovered clock and 600 fs for the recovered data output. Retiming of the data is achieved when the input jitter pulses fall within the switching window of UNI2, which is determined by the almost jitter-free clock pulses. The performance of the circuit has been also tested for various phase misalignments between successive packets and showed similar performance.

Conclusions

In conclusion, we have presented an all-optical, asynchronous, packet CDR circuit. The performance of the overall configuration was tested for 10 Gb/s asynchronous data packets and revealed the regenerative properties of the circuit. It requires no high-speed electronics, acquires synchronization within a few bits and minimizes the guard-bands between successive packets to about 8 bits. This scheme is particularly suitable for optical packet switching applications for use in a receiver or as a regenerator.

References

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