ALL-OPTICAL 10 GB/S HEADER REPLACEMENT FOR VARIABLE LENGTH DATA PACKETS

D. Tsiokos (1), E. Kehayas (1), G.T. Kanellos (1), L. Stampoulidis (1),
G. Guekos (2), and H. Avramopoulos (1)
1: Department of Electrical and Computer Engineering, National Technical University of Athens,
Zographou, GR 15773, Athens, Greece
E-mail: dtsiokos@cc.ece.ntua.gr
2: Swiss Federal Institute of Technology Zurich, ETH Hoenggerberg, CH-80923 Zurich, Switzerland

Abstract *We present an all-optical circuit that performs header separation and insertion to 10 Gb/s variable length optical packets using a packet clock recovery circuit to control a 2x2 optical exchange bypass switch.*

Introduction

Packet switched networks offer the potential for better capacity utilization and higher throughput. To avoid contention and packet loss, packet switches require input/output buffers and with electronics this is relatively easy to implement. Unfortunately for optical packet switching, the implementation of optical buffers is complex and only short buffer depths can be achieved with realistic lengths of optical fibers. To address this issue and to design optical packet switched networks that ensure lossless communication, minimum pre-transmission delay, correct packet order arrival, while needing small buffer requirements, alternative protocols such as the virtual circuit deflection (VCD) protocol have been proposed [1]. In this, if an intermediate link has insufficient capacity for the total incoming traffic, an alternative route is selected for part of it. The alternative route may be selected in a deterministic way and in this case a new, but in-advance known header must be substituted to the incoming packet. Header substitution is a relatively simple operation and thus ideally suitable to be handled in the optical domain, so as to avoid o/e/o conversions. So far, several all-optical techniques have been proposed for header erasure and re-insertion [2], label swapping [3], while 2x2 switches have been demonstrated for the deflection of optical packets to the appropriate outgoing links [4].

In the present communication we demonstrate an optical circuit that performs simultaneously old header separation and new header insertion in 10 Gb/s variable length data packets. The module employs a packet clock recovery circuit, comprising of a Fabry-Perot filter (FP) and an Ultrafast Non-linear Interferometer (UNI) [5] and a cascaded 2x2 UNI-based optical exchange-bypass switch [6]. The former is used to generate a local clock signal of similar duration to that of the original packet, while the latter is driven by the generated clock and performs the task of header separation and re-insertion. The proposed scheme can handle packets of variable length and requires short guardbands.

Concept & Experimental Setup

Fig. 1 shows the experimental setup consisting of three subsystems; the optical packet/header generator, the packet clock recovery circuit and the exchange-bypass switch. A DFB laser diode (LD1) was gain switched at 1.25 GHz to provide 8.8 ps pulses at 1549.2 nm after linear compression. The generated pulse train was modulated using a Li:NbO_3 amplitude modulator (MOD1) so as to form a 2^7-1 PRBS at 1.25 Gb/s and was three times bit-interleaved to produce 10 Gb/s pseudorandom data patterns. At the output of the 8x rate multiplier, modulator MOD2 was used to form packets with fixed length headers and variable length payloads and MOD3 was used to form the new local headers.

The data packet signal was split into two parts in a 50:50 coupler. One part was fed into the packet clock recovery circuit and the other was inserted into the 2x2 exchange-bypass switch. The packet clock recovery circuit consisted of a FP filter followed by a UNI gate [5]. The FP filter was used to partially fill the '0's of the incoming packet providing a clock resembling signal with high amplitude modulation. Its free spectral range (FSR) was equal to the line rate and its finesse was 20.7. The resulting amplitude modulated signal at the output of the filter was used as the control signal in the UNI gate and had its modulation removed by using the nonlinear transfer characteristics of the gate. The gate was designed for 10 Gb/s operation, used a 1.5 μm bulk SOA and was powered by a CW signal at 1545 nm, generated by a second DFB laser (LD2). For the header replacement task to be performed, the recovered clock was fed

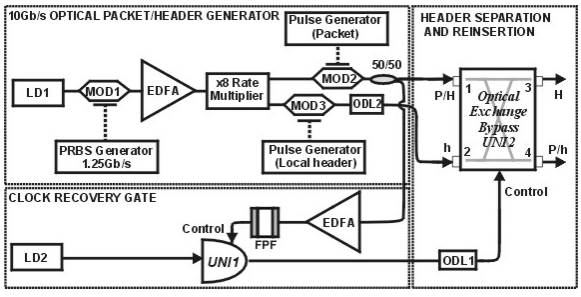

Figure 1. Simplified Experimental Setup

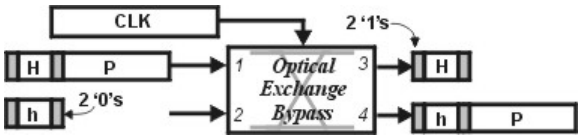

Figure 2. Concept and bit synchronisation scheme

as the control signal into the exchange-bypass switch, while the original data packets and the new, locally generated headers were used as the two inputs. The 2x2 switch is a specially configured SOA-based UNI gate having two input and two output ports [6]. The signals in the 2x2 switch were synchronized with variable optical delay lines ODL1 and ODL2.

Fig. 2 shows a schematic diagram of the proposed concept. The original packets and the locally generated headers were synchronized at the input of the 2x2 switch, whereas the recovered clock used as the control signal was delayed by a time interval corresponding to the header length. Hence, the switch operated in the bar state for the two header sections (H) and (h) and in the cross state for the payload section (P), since only the payload bits fall within the switching window of the control signal. As a result, the initial header (H) was dropped and exited through port 3, while the payload section with its new route information (h) appeared at port 4. The grey fields at both front and end of the header section depict the required guardbands for this operation as determined by the characteristics of the packet clock recovery circuit. Two '1' bits in the leading edge were used to assist the clock extraction process and two '0' bits were used at the trailing edge to avoid switching with the first two imperfect bits of the extracted clock.

Results

A data stream comprising of short unequal packets was produced to test the system performance at 10 Gb/s. Fig. 3(a) illustrates two consecutive packets of 4.4 ns and 6.6 ns width respectively, incident at the exchange-bypass switch (port 1) and the clock recovery circuit. Fig. 3(b) illustrates the new, locally generated headers (h1, h2) as inputs to port 2 of the exchange bypass switch. The corresponding extracted packet clocks as delayed for operation of the 2x2 switch, are shown in fig. 3(c). Both packet clocks display 2 bits rise time and 8 bits fall time. Fig. 3(d) displays the original headers of the two packets dropped at port 3. Finally fig. 3(e) illustrates the switched payload sections attached to their new headers as they appear in port 4.

For the clock recovery operation the circuit required 0.9 mW of CW optical power and 100 fJ of control pulse energy. The pulse energies required for operation of the exchange-bypass switch were 3 fJ for the input signals, and 9 fJ for the control signal. The crosstalk for the bar and cross states of the

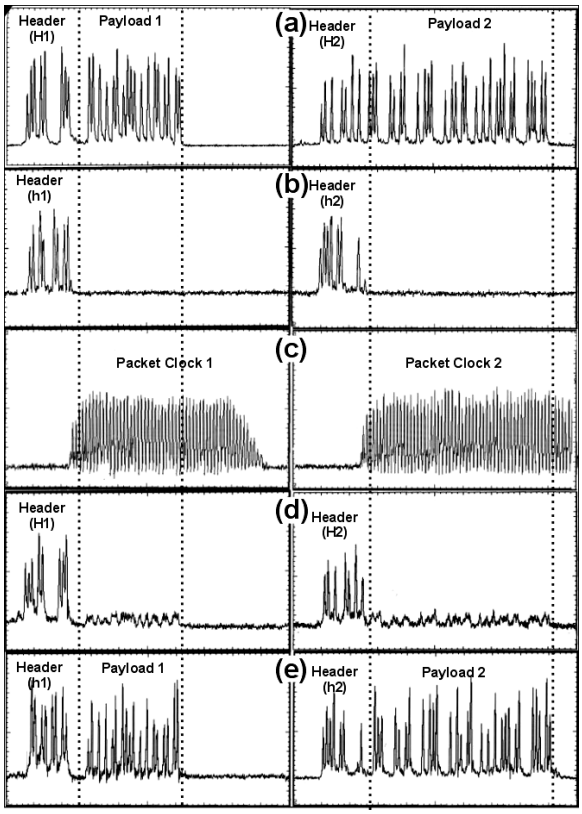

Figure 3. Experimental results for 4.4 ns and 6.6 ns packets. The timebase is 800 ps/div.

exchange-bypass switch was approximately -7 dB and -9 dB respectively.

Conclusions

We have demonstrated an all-optical header separation and re-insertion circuit. The circuit can be used in optical packet switched network architectures designed for low buffer requirements such as virtual circuit deflection routed optical networks. A FP filter and a UNI gate was used for packet clock recovery controlling a 2x2 exchange-bypass switch to perform header replacement. The module was tested using short packets of variable length at 10 Gb/s. The circuit requires short guardbands to operate and does not need any high speed electronics.

References

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