# All-Optical Burst-Mode Receiver at 10 Gb/s

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***Abstract*** *We present the first all-optical 10 Gb/s burst-mode receiver consisting of a semiconductor optical amplifier performing 16 dB amplitude equalization between short bursty packets and two non-linear optical gates performing clock and data recovery.*

## Introduction

Burst-mode reception is a critical and demanding functionality required at the receiver-end of optical packet-switched (OPS) networks in order to successfully retrieve the transmitted packet-formatted information. The bursty nature of the data packets in such networks requires the presence of a burst-mode receiver with a large dynamic range and low lock-in time, being capable to handle the arriving packets instantaneously [1]. To this end, burst-mode reception is typically completed in three stages; amplitude equalization, clock recovery and data recovery. Although all-optical techniques for extracting the clock [2] and recovering the data [3] have been shown to possess great advantages towards the realization of OPS networks with finer granularity, burst-mode reception is still performed in the electrical domain and no all-optical burst-mode receiver has yet been reported. Electronic implementations of burst-mode receivers reported so far [4-6], require a few preamble bytes for successfully achieving amplitude equalization and phase recovery, with the most recent circuit [6] operating at 10 Gb/s and exhibiting 9.2 dB power fluctuation tolerance.

In this article we demonstrate, for the first time to our knowledge, an all-optical burst-mode receiver circuit operating with 10 Gb/s short, asynchronous optical packets with large power variation. The circuit employs a Semiconductor Optical Amplifier (SOA) biased in the saturated regime for achieving packet-to-packet power equalization and a low-Q Fabry-Perot (FP) filter followed by two non-linear optical gates for recovering the clock and data on a packet-by-packet basis. The proposed circuit exhibits 16 dB dynamic range, has a lock-in time of 2 bits and requires 8 bits inter-packet guardbands. Since these guardbands are bit-rate independent [3] and given that optical gates can operate beyond 100 Gb/s [7], the circuit has great potential for use in future high-speed OPS networks with efficient capacity utilization.

## Experiment

The experimental setup is depicted in Fig. 1 and consists of the burst packet generator, the power equalization stage and the packet clock and data recovery circuit. The optical signal was generated by a DFB laser diode (LD1) at 1549.2 nm, gain switched at 9.95328 GHz to provide 9 ps pulses after linear compression. This pulse train was modulated by a $2^7$-1 PRBS pattern in a Ti:LiNbO$_3$ modulator (MOD1) to provide a pseudo-random data pattern at the line rate. A second Ti:LiNbO$_3$ modulator (MOD2), driven by a programmable pulse generator, was used to modulate this data stream into synchronous packets of adjustable length and period. The data packets were time-multiplexed in the asynchronous split-and-combine fiber packet flow generator, designed to provide a differential delay between the two optical paths. Fine phase adjustment of the packets was achieved using a variable optical delay line inserted in one path of the flow generator. The generated data bursts were then fed into the SOA acting as the power equalization unit. Part of the signal obtained at the output of the SOA was inserted into the clock recovery circuit consisting of a low-Q FP filter with free spectral range equal to the line rate and finesse equal to 20.7 and an Ultrafast Nonlinear Interferometer (UNI) gate (UNI1) powered by a CW signal at 1550.5 nm. The second part of the amplitude equalized data packets was used as the input signal in a second UNI gate (UNI2) that serves as the decision element in the data recovery stage and is configured to perform a Boolean AND operation between the data packets and their corresponding clock packets obtained at the output of UNI1 [3]. All SOAs used were 1.5mm bulk ridge waveguide devices with 27 dB small-signal gain and 80 ps recovery time, when driven with 700 mA.

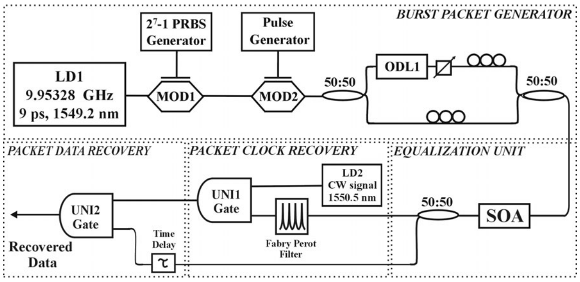

*Figure 1. Experimental Setup*

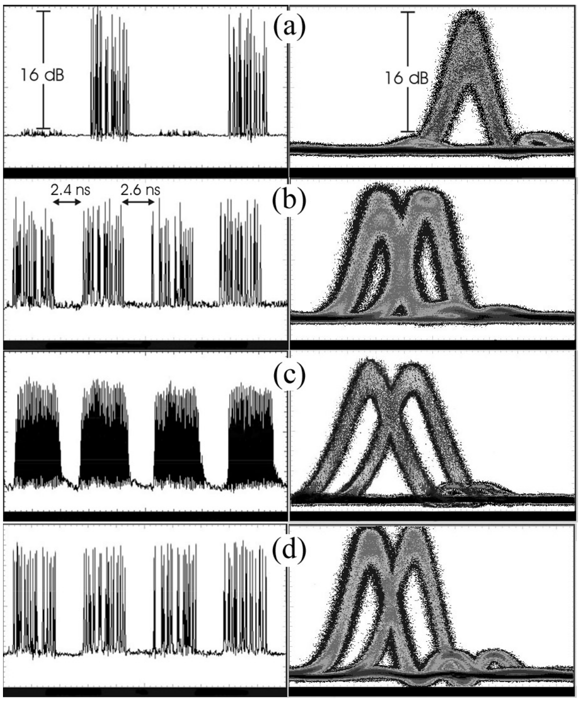


*Figure 2: Oscilloscope traces (2.5 ns/div) and eye diagrams (10 ps/div) of (a) bursty packets, (b) equalized packets, (c) recovered clock packets and (d) received packets*

**Results**

A burst packet stream consisting of packets with adjustable power variation, phase alignment and length was used to test the performance of the system at 10 Gb/s. Fig. 2(a) indicates a sequence of four 40-bit long bursty packets with 2.4 ns and 2.6 ns spacing and 16 dB power variation between successive packets with its corresponding eye diagram. Entering the power equalization stage, the power-varying packet stream invokes a non-linear amplification response in the SOA depending on the specific packet power levels; higher power packets saturate the SOA and result to power-level clipping, while lower power packets experience amplification. In this way, effective power equalization between the packets is obtained at the output of the SOA, as shown in Fig. 2(b). Fig. 2(c) shows the recovered clock packet stream at the output of UNI1 having a sharp rise time of only 2 bits and duration similar to the corresponding data packets [3]. The eye diagram of the self-extracted packet clock signal shown, verifies the improved clock pulse quality in terms of timing and amplitude jitter. Burst-mode reception is completed in the UNI2 gate by using the self-extracted clock packets as the triggering signal and their corresponding data packets as the input signal. Fig. 2(d) shows the received data packets and eye diagram obtained at the output of UNI2, verifying that the received data are effectively amplitude equalized and retimed compared to the original input data. The timing jitter performance of the circuit was further

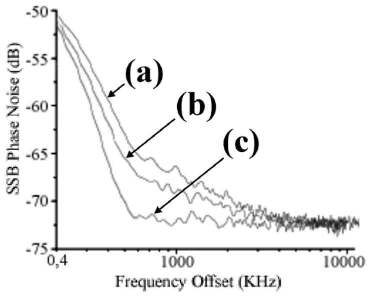


*Fig. 3. SSB spectra at 40GHz of (a) input, (b) received output data and (c) recovered clock*

investigated using a 40 GHz photodiode and a 50 GHz microwave spectrum analyzer in order to calculate the single sideband (SSB) phase noise of the fourth harmonic component as shown in Fig. 3. By integrating the SSB power spectrum over a frequency range between 400 Hz and 10 MHz, the rms timing jitter was found to be 1.6 ps for the original input data, 700 fs for the recovered clock and 920 fs for the recovered data output. Similar performance of the circuit was obtained by varying the phase alignment and the power variation between the data packets from 0 to π and 3 dB to 16 dB, respectively. The average power of the power-varying data signal before the SOA was 600 μW, whereas the switching power and the mean energy per pulse for the CW and the control signal in UNI1 were 0.77 mW and 100 fJ, respectively. The pulse energies for the two signals interacting in UNI2 were 10 fJ for the packet flow and 36 fJ for the recovered clock.

**Conclusions**

We have presented the first all-optical burst/packet mode receiver operating at 10 Gb/s. The circuit has a dynamic range of 16 dB, a fast lock-in time of only 2 bits and requires just 8 bits as guardbands between packets. These bit-rate independent guardbands assure improved bandwidth efficiency for high-speed all-optical packet-switched networks.


**Acknowledgements**

This work was performed within the frame of the European COST collaboration, Action L88. We thank the Swiss Federal Office for Education and Science for the support.


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