Table 1: Optimised parameters for 16-APSK(2,8)

<table>
<thead>
<tr>
<th>SNR(dB)</th>
<th>$A$</th>
<th>$\alpha$</th>
<th>$(P_{90} = 0.1, P_{90} = r4)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>-2</td>
<td>0.842</td>
<td>2.0</td>
<td>(0.740 0.260)</td>
</tr>
<tr>
<td>4</td>
<td>1.457</td>
<td>2.4</td>
<td>(0.713 0.287)</td>
</tr>
<tr>
<td>10</td>
<td>2.764</td>
<td>2.2</td>
<td>(0.578 0.422)</td>
</tr>
<tr>
<td>15</td>
<td>5.170</td>
<td>2.0</td>
<td>(0.543 0.457)</td>
</tr>
</tbody>
</table>

To compare bounds with the coherent channel capacity, the following normalisation is adopted:

$$C_{nc} = \max \{L_n\} \left[ \frac{L_e}{L_n} \right]$$  (7)

where $L_n$ equals $(L - 1)$ or $L$ if differential encoding is used or not.

Results for 16-APSK(2,8) with $L_n = (L - 1)$ and $L_n = L$ are shown in Figs. 1 and 2, respectively. Solid lines represent results for upper bounds while dashed lines represent these for lower bounds. As increases, the bounds come closer together over a broad range of SNRs (the difference between the upper and lower bounds is less than 0.1 bit/symbol). In addition, for $L = 32$, the bounds become close to the coherent channel capacity. Therefore, we can conclude that the coherent capacity is approached. Moreover, a comparison of both Figures indicates that the coherent channel capacity is approached faster with the use of differential encoding.

Fig. 1 Bounds on blockwise noncoherent 16-APSK(2,8)/AWGN channel capacity for $L_n = (L - 1)$

$\circ L = 2$
$\square L = 8$
$\ast L = 32$

- 16-APSK(2,8)/AWGN coherent channel capacity

Fig. 2 Bounds on blockwise noncoherent 16-APSK(2,8)/AWGN channel capacity for $L_n = L$

$\circ L = 2$
$\square L = 8$
$\ast L = 32$

- 16-APSK(2,8)/AWGN coherent channel capacity

D.C. Cunha and J. Portugués (Department of Communications, School of Electrical and Computer Engineering, State University of Campinas—UNICAMP, PO Box 6101, CEP: 13083-852, Campinas-SP, Brazil)

E-mail: dceunha@decom.fee.unicamp.br

References

Jitter reduction in 40 Gbit/s all-optical 3R regenerator using integrated MZI-SOA switches

D. Tsikos, P. Bakopoulos, A. Poustit, G. Maxwell and H. Avramopoulos

Root-mean-square-square-phase jitter reduction from 4 to 1 ps in an all-optical 3R regenerator module operating for continuous and different length data packets at 40 Gbit/s is presented. The circuit is based on hybrid integrated Mach-Zehnder interferometric switches. Error-free operation is demonstrated with 2.5 dB power penalty improvement.

Introduction: The challenge of exploiting more efficiently optical fibre capacity has driven research efforts towards all-optical packet switched networks and systems. To that end, the replacement of electronics by all-optical systems and subsystems is seen as a major milestone that will increase network capacity by handling short IP-like data packets at 40 Gbit/s or higher and will reduce hardware cost by avoiding the use of optoelectronic converters. 3R (re-amplification, re-timing, re-shaping) regenerators appear to be the first network components that will have to be implemented by all-optical technology owing to their broad deployment in network routers, terminals and transmission links for counteracting transmission impairments. In practice, the condition that will bring all-optical 3R regenerators closer to reality is twofold. All-optical 3R regenerators should be capable of regenerating highly degraded signals in order to increase regeneration-free transmission distance, while they should be implemented with integrated, small-footprint, generic devices to eventually facilitate the integration of the regenerator on a single chip. Optical 3R regeneration at 40 Gbit/s has been reported by employing electroabsorption modulators and highly nonlinear fibre [1], or a semiconductor optical amplifier (SOA) with a Mach-Zehnder interferometer (MZI) [2]. Yet in these cases, a high-frequency electrical circuit has been employed for the clock acquisition, in which case an optoelectronic conversion becomes inevitable. An optically-clocked 40 Gbit/s 3R regenerator has been proposed in [3] where regeneration is accomplished through a self-pulsating laser and an MZI switch.

In this Letter we demonstrate a true all-optical 3R regenerator operating for both continuous data flow and short data packets of different length at 40 Gbit/s, which reduces rms phase jitter from 4 to 1 ps and is entirely composed of hybrid integrated MZI-SOAs in terms of active elements. The proposed design involves a wavelength converter (WC), a clock recovery (CR) and a decision element in cascade. The
data and clock remain in the optical domain, thus no optoelectronic converters are required.

![Fig. 1 Experimental setup](image)

**Experimental description**: The experimental setup consists of the 40 Gbit/s optical packet generator, a hybrid integrated MZI-SOA operated as a wavelength converter, the 3R regenerator circuit employing a fibre Fabry-Perot filter (FFP) and two hybrid integrated MZI-SOAs, and the 40-10 demultiplexing circuit as shown in Fig. 1. The original pulse train was produced by a semiconductor mode-locked laser (MLL) operating at a repetition rate of 10 GHz and at a wavelength of 1556 nm. An electrical circuit was employed to introduce sinusoidal phase variation of the generated 4 ps optical pulses through a variable electrical phase shifter driven by a 10 MHz function generator [4]. The jittered signal was used for mode-locking the semiconductor laser and also to drive the demultiplexing circuit for 10 Gbit/s channel demultiplexing. Optical data (2^7-1 PRBS) was generated by a LiNbO_3 electro-optic modulator driven by a 10 Gbit/s pattern generator. A fibre-based bit-interleaver was used to multiply the data rate to 40 Gbit/s, and different length data packets were generated by modulating the 40 Gbit/s data stream with an electro-absorption modulator (EAM 1), which was, however, disabled when testing the circuit for continuous data operation. The 40 Gbit/s test signal was then split and fed to the WC section as well as to the decision gate of the regenerator.

The signal was wavelength converted to 1548 nm through the first MZI, where a push–pull control scheme for high-speed operation. The differential delay of the control signals was optimised by means of an optical delay line (ODL) in order to minimise the switching window of the device and 7 ps pulses were obtained at its output. The WC adds stability to the circuit by applying local parameters to the incoming packets, such as polarisation phase and, potentially, wavelength [5]. The wavelength converted signal was then amplified and injected into the CR circuit to achieve all-optical timing extraction. The CR employed a low-Q fibre FFP filter with free spectral range (FSR) equal to the line rate (40 GHz) and finesse of 39, as well as an integrated Mach–Zehnder interferometer (second MZI) powered by a CW signal at 1552 nm (LD 2), operating as a holding beam. The FFP filter acts as a passive optical resonator that extracts the line rate spectral component of the input signal, transforming the data packets into clock packets with coarse amplitude modulation and duration similar to the corresponding input, as a result of the exponentially decaying impulse response of the filter [6]. This clock-resembling signal entered the nonlinear switch, which acted as a power limiter saturated by the CW light. A push–pull configuration was adopted in order to reduce the switching window, thus obtaining 9 ps clock pulses.

The recovered clock was then used as the input signal to the third MZI, where the incoming data served as the two differential controls. Through a simple logical AND operation, the incoming information was imprinted on the low phase and amplitude jitter clock pulses at the output of the switch.

Finally, in order to measure the bit error ratio (BER) for each multiplexed 10 Gbit/s channel, an EAM (EAM 1) setup was built for demultiplexing each channel. The switching window of the demultiplexer was achieved by combining the electrical jittered 10 GHz sinusoidal signal and a 20 GHz component obtained through an RF frequency doubler and a 20 GHz microwave filter.

**Results and discussion**: The proposed circuit was tested with 40 Gbit/s data in both continuous and packet operation. Initially continuous data at 40 Gbit/s were injected into the 3R regenerator by operating EAM 1 in transparent mode. Fig. 2 shows the evolution of the signal quality through eye diagrams obtained at each stage of the circuit. Fig. 2a shows the highly degraded incoming signal which is then wavelength converted to that shown in Fig. 2b. Fig. 2c shows the clock signal generated after the clock recovery stage, which clearly demonstrates the reduction of both amplitude and phase jitter. The same improvement is demonstrated at the regenerated signal shown in Fig. 2d, since it has been imprinted on the good quality clock pulses.

![Fig. 2 Eye diagrams for 40 Gbit/s continuous data through each stage of circuit](image)

The 3R regenerator performance was also tested with short packets of data of different durations and the results obtained are summarised in Fig. 3. In particular, the oscilloscope traces of the incoming degraded 40 Gbit/s packets are illustrated in parallel to the respective eye diagrams. The incoming packet lengths are 3.6 and 1.6 ps for the left-hand side and the right-hand side packet, respectively. The recovered clock packets were obtained at the output of the clock recovery stage, ensuring clock persistence for duration equal to the corresponding data packet length in addition to 100 ps of rise time (lock-in time) and 350 ps of falltime. The same values were measured for the small packet. The regenerated data packets are obtained at the output of the third MZI, as shown in Fig. 3 with the respective eye diagrams. The MZIs pulse (control: push–pull) energy requirements were 200–100, 300–250 and 90–20 fJ for MZI1, 2 and 3, respectively, confirming femtosecond range operation. Input signal requirements were measured as 6.5 and 6.6 dBm for the CWs of MZI1 and 2, respectively, and 100 fJ of pulse energy for MZI3.

![Fig. 3 Results obtained with data packet operation of 3R regenerator](image)

Significant phase jitter reduction was confirmed by integrating the single sideband (SSB) noise spectra from offset frequency of 1 kHz to 10 MHz on the second microwave harmonic of the demultiplexed
Conclusions: We have presented a true all-optical 3R regenerator for continuous as well as different length optical packets of 40 Gbit/s data, which is based on hybrid integrated MZI-SOA switches. The phase jitter has been reduced from 4 to 1 ps while a power penalty improvement of 2.5 dB was obtained for the regenerated signal. The recovered clock and data remain in the optical domain, thus the need for post-optical conversions is dispensed with. Three identical small-footprint integrated MZI-SOAs were employed, constituting the first step towards the integration of the entire 3R regenerator as targeted by the IST-MUFINS project [7].

Acknowledgment: The authors acknowledge EC support under project 004222/MUFINS of the FP6-IST programme.

© The Institution of Engineering and Technology 2006
3 May 2006
Electronics Letters online no: 20061383
doi: 10.1049/el:20061383

D. Tsioskos, P. Bakopoulos and H. Avramopoulos (Photonics Communications Research Laboratory, National Technical University of Athens, 9 Iroon Polytechniou Street, Zografou 15773, Athens, Greece)
E-mail: dtsioskos@mail.ntua.gr
A. Poustie and G. Maxwell (Centre for Integrated Photonics, Adastra Park, Ipswich IJP 3RE, United Kingdom)

References
3 Slovak, J., Bornholdt, C., and Sartorius, B.: ‘All-optical 3R regenerator for asynchronous data packets at 40 Gbit/s’, Proc. European Conf. on Optical Communications, 2004, We.2.5.7 pp. 388–389
7 http://mufins.cti.gr

500 μm diameter CMOS compatible avalanche photodiodes with 500 MHz bandwidth

A.M. Moloney and A.P. Morrison

Novel silicon-on-insulator, large area (500 μm diameter), CMOS avalanche photodiodes for use with plastic optical fibre are presented. Patterns have been formed on the devices to reduce junction capacitance. Measurements on the patterned devices, at 650 nm and 26 V reverse bias, revealed bandwidths of >500 MHz.

Fig. 1 Cross-section and plan view of standard APD, and plan view of checkerboard pattern and circle pattern APDs

a Cross-section of standard APD
b Plan view of standard APD
c Plan view of checkerboard patterned APD
d Plan view of circle patterned APD

Photodetector design and fabrication: The APDs, which were originally designed for single photon counting, are shallow junction, CMOS compatible devices. Details of the fabrication have been reported in [3]. To reduce the effects of slow carrier diffusion and increase speed, the devices were fabricated on SOI substrates having a 5 μm high resistivity top silicon layer and a 5000 Å buried oxide. Figs. 1a and b show a cross-section and plan view of the APD. The n+ region extends beyond the p+ region (by an amount known as the overlap) forming a virtual guardring, which helps 500 μm diameter active areas and 5 μm overlaps. The active areas of some of the diodes were patterned to reduce junction capacitance. Figs. 1c and 1d show the two types of patterns used. The first is a checkerboard pattern, formed from 10 μm squares of p+ enrichment separated by 2 μm spacings. The second is a circle pattern, formed from 10 μm diameter circles of p+ enrichment.

Results: Initially wafer level capacitance-voltage (C-V) measurements were made on the three diodes. A HP4280A 1 MHz C-V plotter was used for the measurements. The results were adjusted to allow for the ∼0.5 PF capacitance arising from the 100 μm square bondpads. Fig. 2 plots capacitance against voltage. Clearly, the standard diode has the highest junction capacitance and the circle patterned diode has the lowest. The reduction in junction capacitance from the standard diode to the circle patterned diode varies from ∼1–2 PF at biases close to breakdown (27–30 V) to a maximum of ∼30 PF at 0 V. The decrease in junction capacitance is obviously due to a decrease in active area since the checkerboard and