

Characterisation of Hybrid Integrated All-Optical Flip-Flop

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Abstract- We present a fully-packaged, hybrid-integrated all-optical flip-flop with separate optical set and reset operation. The flip-flop can control a wavelength converter to route 40 Gb/s data packets all-optically. The experimental results are given.

I. INTRODUCTION

The mismatch between the fiber transmission bandwidth and router forwarding capacity has led to extensive investigation on all-optical packet switching [1-3], where switching, routing and forwarding are carried out in the optical domain. Examples of optical packet switches are shown in [1, 2], where the flip-flop acts as an optical element to store the switch control information. The flip-flop state is determined by the processed packet headers, and the flip-flop in its turn controls a wavelength converter to route the data packet to a specific port. Previous all-optical flip-flops are demonstrated using discrete devices [4], which suffer from a complex set-up involving multiple fibre pigtailed, or using monolithic InP based designs [5, 6] that have high optical losses and are difficult to package. Importantly, these issues become limiting factors when scaling the devices for multiple channels. Hybrid integration offers cost effectiveness for multi-channel packaging [7]. It also provides inherent path length stability, low-loss capability. In this paper we present a fully packaged hybrid-integrated all-optical flip-flop based on two coupled Mach-Zehnder interferometers (MZIs). We demonstrate that the flip-flop is capable of driving a wavelength converter to all-optically route 40 Gb/s data packets.

II. OPERATION PRINCIPLE

A schematic of the device layout is shown in Fig. 1. It consists of two coupled MZIs. Each MZI has a semiconductor optical amplifier (SOA) in one arm. A laser emits a continuous wave (CW) bias light at wavelength λ_1 that is fed into a MZI 1. The MZI 1 output is sent into MZI 2, which has the same structure, but biased by a CW light with a different wavelength, λ_2 . The system has two possible states. In State 1, the MZI 1 output suppresses output from MZI 2, so λ_1 dominates the output. In State 2, the MZI 2 output suppresses output from MZI 1, and then λ_2 is dominant. The operation principle can be briefly

explained as following [4, 6]. When the CW light with λ_1 is injected into MZI 1, MZI 1 is set such a way that the light out of MZI 1 goes mostly into the low branch of the 50/50 coupler output. This light then flows into MZI 2 via the 50/50 coupler in MZI 2, and affects the gain and phase shift that light sees flowing through it. The MZI 1 light perturbs the SOA 2 properties such that the CW bias 2 light (λ_2) flowing through SOA2 and phase shifter 2 goes mostly into the top output of the 50/50 coupler in MZI 2. Then the CW bias 2 light (λ_2) does not travel into the MZI 1, and does not affect the properties of SOA1. In effect, the MZI 1 output suppresses output from MZI 2. As the system is symmetric, it is also possible that MZI 2 suppresses output from MZI 1. The states of the system can be switched by sending a light pulse (via Set or Reset port) into the MZI that is currently dominant. This light will switch the MZI output away from suppressing the other MZI, allowing the other MZI then to become dominant.

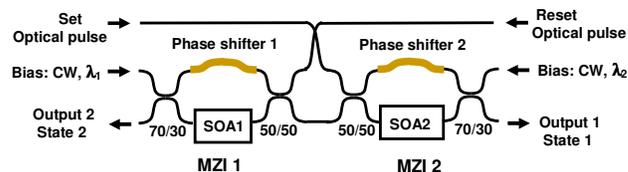


Fig. 1: Schematic diagram of the optical flip-flop memory.

III. DEVICE DESIGN

The device (fabricated by CIP) was designed on a silica on silicon, passive assembly, hybrid integration platform (motherboard) incorporating $\Delta=0.75\%$ buried channel, single-mode silica waveguides with transmission losses of $<0.1\text{dB/cm}$ [7]. These waveguides formed the basis of the optical circuitry depicted in Fig. 1. The SOAs were mounted onto separate silicon submounts and flip-chipped into precision recesses milled in the silica on silicon motherboard. Typical SOA coupling losses were $<1.5\text{dB}$. Fibre pigtailed were also located onto separate silicon submounts and flip-chip integrated onto the motherboard. The chip design including integration features is shown in Fig. 2, which depicts two complete flip-flops on one chip. The size of the chip is about

45 x 12 mm². The whole device was fully packaged into one complete module including Peltier coolers for both SOAs and thermo-optic silica waveguide phase shifters.

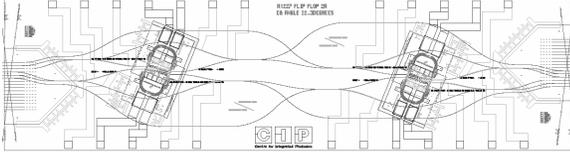


Fig. 2: Planar silica waveguide layout of the optical flip-flop memory. This layout shows two flip-flop devices (separated vertically).

IV. EXPERIMENTAL RESULTS

The CW bias wavelengths for λ_1 and λ_2 were set at 1562nm and 1565nm with input powers of 3dBm and 6dBm respectively. SOA1 and SOA2 were temperature controlled to 22°C and biased at 122mA and 76mA respectively. By toggling the flip-flop manually (static measurement) the device switched from State 1 to State 2. The spectral output at each memory state was measured by an optical spectrum analyser and is depicted in Fig. 3a and 3b, showing contrast ratios of 13dB and 10dB for State 1 and State 2, respectively.

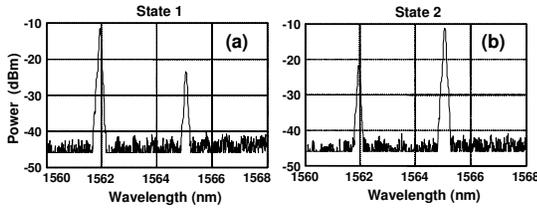


Fig. 3: Spectral output at each state of the flip-flop. (a) represents State 1 (λ_1 dominant), and (b) represents State 2 (λ_2 dominant).

The dynamic operation of the flip-flop was demonstrated by toggling the state of the flip-flop by injecting a sequence of optical pulses into the MZI that was controlling the operating state. The pulses had a wavelength of 1563nm and a pulsewidth of less than 150ps (FWHM). The pulses were injected into both MZIs every 32 ns via the set and reset ports. The temporal results of the output states and the set/reset inputs are shown in Fig. 4. In Fig. 4a, optical pulses are injected into MZI2 via Set port (see Fig. 1) to set the flip-flop to State 1. Fig. 4b shows the optical pulses that are injected into MZI1 via Reset port to set the flip-flop to State 2. The optical peak power of the pulses in Fig. 4a is 5 dBm and 6 dBm in Fig. 4b. Fig. 4c and Fig. 4d present the dynamic output of the flip-flop at Output1 and Output2. The switching between flip-flop states every 32 ns is clearly observed and the flip-flop state is stable in the time between changing states. The switching time is less than 200 ps.

Fig. 5 shows the experimental results of wavelength routing by employing the optical flip-flop. The flop-flop is toggled its state by injecting external set and reset optical pulses. The flip-flop outputs 1559 nm wavelength with 2 ns duration time. This output light controls a SOA-MZI wavelength converter [8] to convert a 40 Gb/s data packet (1.6 ns@1545 nm) to the

flip-flop output's wavelength (1559 nm). The converted packet can be spatially routed into a specific port by using an AWG. It can be seen in Fig. 5 that within the 2 ns duration time, the whole input 1.6 ns data packet is converted into a new wavelength (1559nm). BER measurement shows that the output from flop-flop is comparable to an external tuneable laser. The power penalty is less than 1.5 dB.

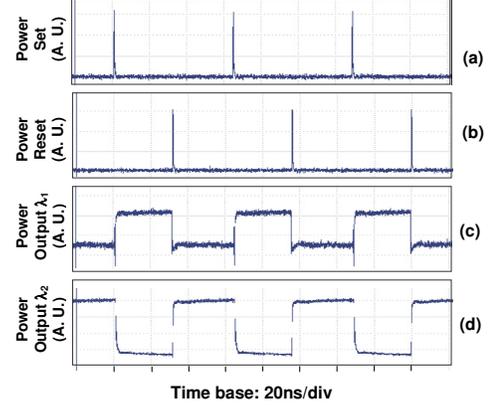


Fig. 4: Dynamic output of the flip-flop showing switching between states every 32 ns. The upper panels (a) and (b) are the traces of the external optical pulses at wavelength 1563 nm. The lower panels (c) and (d) are the dynamic output of flip-flop at each wavelength λ_1 and λ_2 .

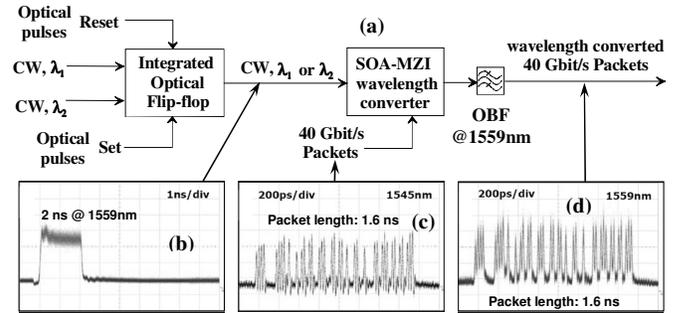


Fig. 5: (a) Block diagram of the wavelength routing, (b) dynamic output from optical flip-flop, output wavelength at 1559 nm with 2 ns duration time, (c) input 40 Gb/s data packet, packet length 1.6 ns, at 1545 nm, (d) wavelength conversion results of 40 Gb/s data packet, at 1559 nm.

V. CONCLUSIONS

A fully-packaged, hybrid integrated all-optical flip-flop memory is demonstrated. We show that the optical flip-flop is capable to control a 40 Gb/s wavelength converter for all-optical wavelength routing.

This work was supported by the EU project LASAGNE (IST-2004-507509).

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