Optical signal processing using integrated multi-element SOA–MZI switch arrays for packet switching

N. Pleros, P. Zakynthinos, A. Poustie, D. Tsiokos, P. Bakopoulos, D. Petrantonakis, G.T. Kanellos, G. Maxwell and H. Avramopoulos

Abstract: The use of discrete but interconnected SOA–MZI switches for performing logical and highly functional processing tasks, demonstrating the multi-functional potential of the photonic switching elements is discussed. An all-optical 3R burst-mode receiver consisting of four SOA–MZI switches and operating error-free with 40 Gb/s optical bursts, proving that interconnection of multiple switching units can lead to the realisation of key network node functionalities offering increased intelligence at the physical layer is presented. In order to allow for easier interconnectivity between the SOA–MZI switches and to provide compactness and cost effectiveness to the developed subsystems, the integration of multiple switches into the same platform is proposed. To this end, the implementation of the first integrated quadruple SOA–MZI switch array is reported, increasing the integration density level and reducing packaging and pigtailing costs. Finally, possible applications of integrated multiple switch arrays are discussed, indicating their suitability for producing compact circuits performing common processing tasks in a multi-wavelength environment, as well as their potential to lead to the development of an all-optical high-speed packet switched node by implementing critical packet switching functionalities in a compact and efficient way.

1 Introduction

The request for high-speed all-optical signal processing has been posed by current and near-future optical networks in an effort to release the network nodes from undesirable latencies and speed limitations imposed by O/E/O conversion stages and to match the processing and transmission speeds. In this respect, a significant increase in research efforts towards the deployment of high-speed all-optical signal processing technology, application concepts and demonstrations has been witnessed during the past few years [1–4]. Semiconductor optical amplifier (SOA)-based, interferometric optical gates have appeared as the main-stream photonic signal processing units [5–9], exploiting their fast response for high-speed operation [10–11] and taking advantage of the remarkable advance of hybrid and monolithic integration techniques [12–14] for offering compact switching elements. To this end, single element, high-speed all-optical gates have been demonstrated as integrated devices [12–16] in a number of laboratories across the world and have been developed as commercial products [17] primarily for wavelength conversion and regeneration purposes. These devices have been utilised in single-gate experiments performing wavelength conversion at rates over 160 Gb/s [18–20] or regeneration with bitwise processing capability in excess of 40 Gb/s [17, 21–25], offering in this way a viable platform for high-speed processing required by future circuit switched nodes. However, much of the research in wavelength conversion and regeneration configurations has focused on continuously increasing the processing speed performance of optical gates, and as such, the logic and functional potential offered by all-optical gates has not been fully explored yet. Several logical elements are required in order to form functional modules that will be able to perform any useful processing task and to reap the advantages of high-speed, bitwise processing. This can be also verified by a number of experiments that exploit multiple interconnected switching elements and demonstrate complex Boolean optical logic functionalities at high data rates [26–28]. In addition, recent research has indicated the suitability of multiple interconnected optical gates in forming the cornerstone of all-optical functional blocks even for demanding packet switching, label switching or burst switching architectures [29–32], where packet-format transparency is targeted. In this context, SOA-based optical gates have served as the key elements in packet- or burst-switched configurations utilising their fast response to external light injection [11] and their strong nonlinear characteristics [33] in order to handle the incoming information irrespective of the precise packet phase alignment, packet duration or packet-to-packet power-level fluctuation. To this end, the interconnection of optical gates has allowed for the realisation of critical functionalities within a packet- or burst-switched node like label/payload separation [34], header processing [35–38], label erasure and rewriting [31], and packet clock and data recovery [39, 40].

Despite their capability to form functional subsystems for packet switching applications, the deployment of an optical node based on integrated photonic switching devices remains still an elusive target. Some of the main reasons for

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this are certainly the bulky circuitry when using interconnected single-element optical gates and the high cost of photonic integration technology and more specifically the high cost associated with packaging. Within this frame, the time has come to take the next logical step in the evolution ladder of all-optical signal processing and to integrate multiple switching elements on a single chip and to interconnect these integrated switching elements into functional logic modules with the aid of a few external components. In this way, cost reduction will be achieved, since the high cost associated with packaging and pigtailing will be shared among all the switches employed on the chip. Moreover, compactness of the circuitry will be enhanced, while at the same time, interconnectivity between the switches will be accommodated, opening the inroad for low-volume functional subsystems capable of performing demanding processing tasks.

In the present communication, we present recent research results obtained within the frame of the European IST-MUFINS project that provide experimental proof of the above argumentation. First, we demonstrate the multifunctionality of multiple interconnected optical gates by implementing a 40 Gb/s 3R burst mode receiver (BMR) circuit that comprises four hybrid integrated, interconnected SOA-based Mach-Zehnder interferometric (SOA–MZI) optical gates [41], each one performing a different processing task. So far, burst mode reception has been realised only by means of electronic or optoelectronic approaches, suggesting that the proposed all-optical BMR circuit is definitively a proper example for demonstrating the enhanced applications of interconnected optical switching elements. Following that, we report on the development of the first integrated quadruple switch arrays with a per switch processing capability of 40 Gb/s [42]. These devices employ four integrated SOA–MZI switches on the same chip, reducing in this way the cost per SOA–MZI, while they prove that integration density increment of photonic switching technology is feasible.

The rest of the paper is organised as follows. Section II presents experimental results of the 40 Gb/s 3R burst mode receiver circuit and Section III describes the implementation procedure followed for the development of quadruple MZI switch arrays. Finally, Section IV discusses the applications of integrated multi-element switch arrays emphasising on their suitability for the development of optical packet switched nodes and Section V concludes this article.

2 All-optical 40 Gb/s 3R burst mode receiver circuit

3R burst-mode receivers are required in every optical packet/burst switched node in order to recover or regenerate optical packets/bursts irrespective of their size, their power level and their synchronisation. This reception or regeneration of packet format transparent information imposes the additional requirement for a burst-mode receiver circuit to possess a large input power dynamic range and ultrafast response characteristics. To this end, burst-mode reception is typically completed in a three-stage procedure: power equalisation of the incoming bursts, clock extraction and data recovery (CDR) for every burst separately [43].

So far, mainly electronic or optoelectronic configurations have been proposed and no attempts for 3R burst mode reception directly in the optical domain have been reported. Electronic implementations of burst mode receivers have been demonstrated, operating at 10 Gb/s and requiring a few preamble bits for achieving power equalisation and phase recovery [44–45]. Differential phase shift keying (DPSK) coding schemes have also been utilised in optoelectronic implementations [46] to provide BMRs with enhanced dynamic range. All-optical approaches for the development of CDR circuits [47, 48] and of 2R-burst mode regenerators operating at 40 Gb/s [49] have also been reported, indicating the potential of photonic solutions to reach high data rates. However, these approaches have not been utilised together to form a 40 Gb/s 3R burst mode receiver circuit and so far only configurations for all-optical 3R burst-mode reception at 10 Gb/s have been proposed [50, 51].

This section is dedicated to the demonstration of the first all-optical 3R burst mode receiver circuit operating with 40 Gb/s asynchronous, variable length bursts with intense power variation. The proposed module is based completely upon commercially available, hybrid integrated SOA–MZI switch technology [17], taking advantage of their multifunctional potential. The 3R BMR circuit employs a record number of four cascaded SOA–MZIs each one performing a different functionality. The circuit exhibits an input power dynamic range of 9.3 dB, has a lock-in time of only 5 bits and requires a guard band of 14 bits between packets.

2.1 Experimental setup

The experimental setup is shown in Fig. 1. It consists of the 40 Gb/s optical packet generator, an array of four hybrid integrated SOA–MZIs (HMZI) forming the burst mode receiver (BMR) and an additional HMZI used as a 40–10 Gb/s demultiplexer. The BMR comprises a power-equalisation unit (PE) implemented with a HMZI with unequal coupling ratios, a HMZI wavelength converter (WC) and the clock and data recovery unit (CDR) that employs a fibre Fabry–Perot filter with two HMZIs performing clock recovery and data reception [39, 40]. In order to generate the asynchronous packet traffic, a 1553 nm DFB laser was gain switched at 10.025 Gb/s to produce 7 ps pulses after linear compression. This pulse train was launched into a nonlinear fibre pulse compressor to reduce its pulse width to 3 ps, so as to facilitate bitwise processing in the subsequent SOA–MZI stages. After

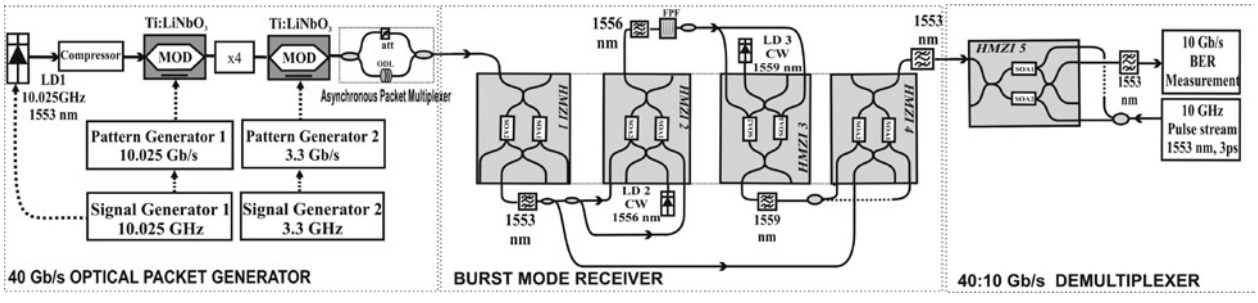

Fig. 1 *Experimental setup. HMZI1 operates as a power equaliser, HMZI2 performs wavelength conversion and HMZI3 and HMZI4 are responsible for the clock-and-data recovery process*

exiting the compressor, it passed through a Ti:$LiNbO_3$ electro-optic modulator driven by a 10.025 Gb/s pattern generator and was multiplexed to 40.1 Gb/s in a fibre bit-interleaver to form a 2^7-1 PRBS data pattern. The output of the fibre multiplexer was launched into a second modulator driven by an electronic pulse-pattern generator to produce data packets of unequal lengths. This packet stream was then introduced in the asynchronous split-and-delay packet flow generator that consists of a 3 dB coupler with fibre lengths at its output, to provide 250 ns of differential delay between the two paths before recombination in a second 3 dB coupler. The bursty traffic obtained at the output of the asynchronous packet flow generator entered as input signal to the power-equalising HMZI1.

HMZI1 had unequal splitting ratios (70/30) at its input and output couplers and was configured to provide self-switching operation for the incoming burst-formatted traffic, by also using different bias currents for its two SOAs [52]. With this arrangement, the optical gain saturation properties of the two SOAs resulted in high gain for the low-power packets and low gain for the high-power packets, delivering nearly power-equalised packets at the output of HMZI1. Moreover, the unequal splitting ratios of the HMZI1 input coupler in conjunction with the different SOA driving conditions (340 against 190 mA) resulted to an approximately π differential phase shift between the packet signal in the two arms of the interferometer before interference in its output coupler. In this way, self-switching operation of HMZI1 was performed and the interference at the MZI output coupler provided nearly background- and noise-free, power-equalised packets at its output. In order to operate successfully, HMZI1 required 129 fJ/pulse for the input signal, corresponding to 229 fJ/pulse for the high-power packet stream and to 29 fJ/pulse for the low-power sequence.

The power-equalised packet stream was then split and one part was fed as the control signal into HMZI2 to perform wavelength conversion and clock recovery, whereas the other part entered as input signal the HMZI4 for data reception. The wavelength converter was used as an interface to assign locally controlled signal parameters for the wavelength and the carrier phase. The new wavelength was required in order to match one of the transmission peaks of the fibre Fabry–Perot filter (FFP) employed in the clock recovery stage, whereas the locally assigned carrier phase of the wavelength-converted signal was used for allowing coherent signal addition in the FFP. As such, the wavelength converter provided at its output a 40 Gb/s data signal at 1556 nm with a pulse width of 7 ps. The wavelength-converted signal was then amplified and injected into the clock recovery (CR) module to achieve all optical timing extraction. The CR employed a low-Q FFP filter with free spectral range (FSR) equal to the line rate (40.1 GHz) and a finesse of 39, followed by HMZI3 that was powered by a CW signal at 1559 nm (LD3). The FFP filter transformed each data packet into a clock signal with duration similar to the respective input packet but with intense pulse-to-pulse amplitude modulation. This clock-resembling signal entered the following HMZI3 switch that operates as a power limiter [53], yielding a power-equalised clock packet stream at its output [41]. HMZI3 was used in a push–pull control configuration to reduce its switching window and to provide 7 ps clock pulses. Data recovery on a per packet basis was completed in HMZI4 by using the power-equalised packets as input and their corresponding recovered clock packets as triggering signal, reducing in this way the timing jitter and the amplitude modulation of the input signal [54]. Finally, HMZI5 was used as a 40:10 Gb/s demultiplexer using a 3 ps clock pulse stream as the control signal in a push–pull configuration in order to allow for BER measurements of the received data. The SOAs employed in the HMZIs had a length of 1.1 mm, small signal gain equal to 30 dB when driven with 300 mA dc current, a saturation output power of 6 dBm and polarisation gain dependence less than 1 dB. EDFAs were used in-between interconnected HMZI stages to compensate for signal's propagation losses.

2.2 Experimental results

By changing the width, period and delay of the electrical pulse train driving the second modulator, data packets of various length, period and data content were generated in order to test the performance of the BMR circuit. Fig. 3 illustrates the evolution of the burst mode reception process through oscilloscope trace and eye diagrams obtained at each stage of the circuit. Fig. 2*a* shows a typical sequence of four asynchronous incoming data packets at 40 Gb/s having a size of 48 and 75 bits, respectively, and exhibiting power fluctuation of 9.3 dB. Fig. 2*b* shows the respective power-equalised packet stream obtained at the output of HMZI1. The 9.3 dB power fluctuation between the incoming packets has been reduced into roughly 2 dB amplitude modulation between the pulses within the power-equalised packets, while the noise '0' level is suppressed. Fig. 2*c* depicts the wavelength converted data signal exhibiting a moderate improvement regarding the amplitude modulation. Fig. 2*d* shows the recovered clock packets obtained at the output of the clock recovery stage. They persist for time duration that equals that of the corresponding input data packet extended by a 14 bit decay time on its trailing edge. This value determines the time required by the CR signal to decay to 1/e after each packet. In addition, the recovered packet clocks exhibit a 5 bit rise time at their leading edge, which is the

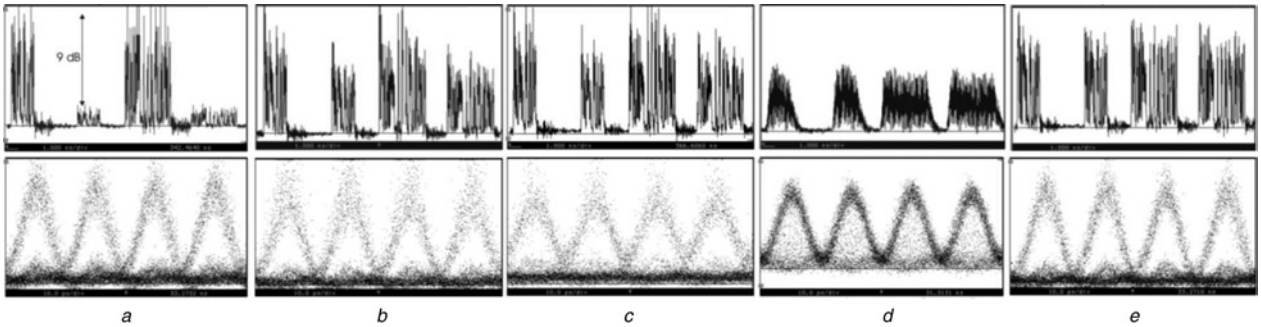

Fig. 2 *Oscilloscope traces and eye diagrams for:*
(*a*) input, (*b*) power equalisation unit, (*c*) wavelength conversion, (*d*) clock recovery and (*e*) output signals
Time scale is 1 ns/div for the oscilloscope traces and 10 ps/div for the eye diagrams

Table 1: Power/energy requirements of MZI switches

MZI	Input	Control	
		Push	Pull
MZI1 (PE)	129 fJ		
MZI2 (WC)	7.6 dBm (CW)	107 fJ	49 fJ
MZI3 (CR)	0 dBm (CW)	100 fJ	65 fJ
MZI4 (AND)	47 fJ	359 fJ	143 fJ
MZI5 (DEMUX)	4 fJ	100 fJ	10 fJ

time required for capturing synchronisation, suggesting the use of the first 5 bits in the data as preamble in order to avoid information loss. In addition, the power-level fluctuations of the rise and decay pulses appear as hits inside the eye diagram of the extracted clock, yielding a closed eye waveform that does not correspond to the real quality of the recovered clock signal. This can be verified by clearer eye opening when the size of the data packets and as such the ratio of the power equalised to the imperfect clock pulses is increased, revealing an intensity contrast enhancement between the dots forming the pulse shape and the dots inside the eye. Fig. 2*e* illustrates the received equalised data packets at the output of the burst mode receiver, indicating clearly that timing jitter and amplitude modulation reduction with respect to the corresponding signal at the output of the PE unit (HMZI1) is obtained. The switching energy/power requirements for all the HMZIs are summarised in Table 1.

Fig. 3 shows BER measurements for all four 10 Gb/s channels. The curve identified as 'BtB 9 dB' shows that it was not possible to obtain error-free measurements of the input packets with the 9.3 dB power fluctuation, reveling an error floor at 10^{-5}. The error floor was eliminated after the power-equalisation stage, as shown by the curve 'PE o/p' and error-free operation could be obtained, indicating that even a single optical gate with unequal coupling ratios and SOA driving currents can perform as a 2R burst mode reception device. Error-free operation was also achieved at the output of the BMR depicted by the curve 'BMRx o/p', with a negative power penalty of 1.95 dB with respect to the power-equalisation stage output. Error rate measurements were also taken for the input packet signal with no power fluctuation, as illustrated by the curve 'BtB 0 dB'. This BER curve lies between the two previous curves and has a 1.3 dB positive power penalty offset with respect to the 'BMRx o/p' curve revealing the 3R capability of the BMR circuit.

3 Photonic on-chip switch arrays

The first milestone on the evolution of all-optical signal processing is reached by verifying that discrete all-optical gates can be interconnected producing all-optical circuits with increased functionality and intelligence like the all-optical 3R burst-mode receiver presented in the previous section. However, the demonstration of burst-mode reception directly in the optical domain was made possible by adopting of a common photonic hybrid integration platform for the development of integrated and compact SOA–MZI switches [55]. This photonic integration platform is a pragmatic combination of the best available optical technologies for active and passive optical devices. The platform is uniquely designed for passive assembly of the different components in order to maintain high optical performance and low insertion losses, but at much lower cost. In a similar method to the electronic printed circuit board used in electronics, a planar

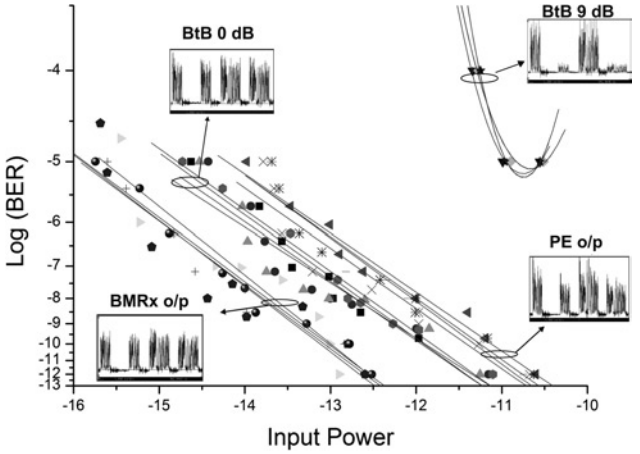

Fig. 3 *Experimentally measured BER results at various parts of the BMR circuit*

silica on silicon waveguide acts as a motherboard to host both active and passive devices. Integration is achieved by plugging precision-machined silicon submounts or 'daughterboards' carrying individual optical components into the motherboard. The individual components have precision-cleaved features for accurate mechanical positioning on the daughterboard. In the case of the development of single-element SOA–MZI optical gates, the daughterboards are designed to host monolithic twin SOA chips and provide all suitable alignment stops. These SOAs are specially designed to have high gain and maximised nonlinearity by incorporating optical mode expanders. The mode expanders enhance the optical performance by reducing the facet reflectivity to $<10^{-5}$ which allows high gain to be maintained at high bias currents. They also facilitate passive alignment by reducing the sensitivity of the coupling loss to misalignment. Fig. 4 shows photographs of photonic integrated prototype devices along with the corresponding motherboard schematic designs. The fully packaged and pigtailed SOA–MZI optical gate is shown in Fig. 4*a*, along with the motherboard design, as shown in Fig. 4*b*. The fibre pigtailing is also achieved with a passive assembly approach using arrays of optical fibres in precision V-grooves on a silicon carrier. The daughterboard depicted in Fig. 4*c* consists of a twin SOA array and is flip-chipped onto the motherboard [17].

This integration technique based on hybrid assembly offers unique advantages in terms of scalability and low daughterboard/motherboard interface losses and as such can be applied equally well to more devices or a large subsystem integrating many component elements. In this context, this technique allows for the integration of multiple switching elements on the same chip, reducing packaging and pigtailing costs and increasing the integration density level, while offering a compact solution for the interconnections needed in order to form functional modules. Fig. 4*d* shows a photograph of the first packaged and pigtailed photonic switching multi-element unit that houses a quadruple array of SOA–MZI optical gates [42]. The corresponding motherboard design is shown in Fig. 4*e* with the two daughterboards clearly marked, each one carrying a quad array of SOAs forming two SOA–MZI optical gates, as illustrated in Fig. 4*f*. In this example, a quad SOA array is chosen as the modular active element because this can now be fabricated at high yield and hence reduced cost. As the monolithic integration technology improves, the number of SOAs on the chip is expected to increase to 8 or 16, with the advantages of reduced footprint and of only one assembly being required for simultaneous alignment of many elements. Adopting a hybrid integration technique also

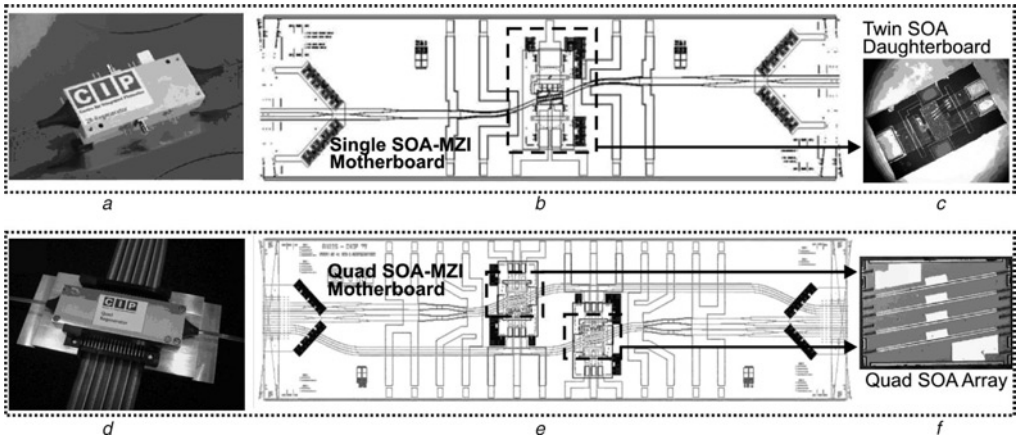

Fig. 4 *Single and quadruple integrated SOA–MZI layouts*

a packaged and pigtailed SOA–MZI optical gate
b corresponding motherboard design and
c twin SOA silicon submounts
d packaged and pigtailed prototype device containing four SOA–MZI optical gates on a single photonic chip
e corresponding motherboard design and
f quad array of SOAs used for constructing each double SOA–MZI gate within the chip

allows these modular active elements to be placed at different physical positions in the circuit, which is required to spread the thermal load on the overall module.

Thermal loading is one of the main issues around increasing integration density of active optoelectronic components because the inherent power inefficiency of optical devices means that excess heat is generated. For example, a single SOA may require a 300 mA current at ~2 V bias, giving a power consumption of 0.6 W, whereas the produced optical power is typically only <0.02 W. The excess heat needs dissipation because today's SOA devices exhibit gain reduction at elevated temperatures. Future advances in new InP materials, such as using Al doping, may relax the requirements of having to cool the SOAs and will make the increased density of active elements more practical. However, for the packaged quad SOA–MZI module shown in Fig. 4*d*, only one Peltier cooling element is required for dissipating the ~5 W generated when all the SOAs are biased simultaneously. There is also heat generated from the thermo-optic phase-shifters on the motherboard (used to control the MZI phase bias) but this can be minimised by trenching the silica at these points in the circuit [56].

Measuring the insertion losses for packaging a quad SOA–MZI module showed that there was no significant increase in the loss when moving to these larger and multiple SOA arrays. This shows that this hybrid integration technique is scalable and should be extendable to larger arrays in the future.

4 Discussion

Multi-element switch arrays on a single chip can also lead to efficient and compact processing modules required by future WDM circuit-switched networks. These devices are capable of performing already demonstrated processing concepts in a multi-wavelength environment, by associating each channel with one of the switches for the implementation of the required process. For example, the integrated quadruple SOA–MZI switch array can be conceptualised as a four-channel processing module providing the possibility for performing four-channel wavelength conversion or four-channel 3R regeneration of continuous data streams [17]. In this context, quadruple switch arrays in cascades could, in principle, also serve as the main building blocks of a four-wavelength burst-mode receiver based on the principle of operation described in Section II. Fig. 5 shows the design of this four-channel BMR incorporating four cascaded switch arrays. Each quadruple switch array is dedicated to a specific processing task for all the wavelengths, whereas each row of the cascaded devices forms a single-wavelength BMR as the one presented in Section II. As such, the first quadruple switch array is used for power equalisation between the optical bursts carried at each wavelength, the second switch array is devoted to perform wavelength conversion and the remaining two switch arrays with the aid of a single, common Fabry–Perot filter form the clock-and-data-recovery stage for

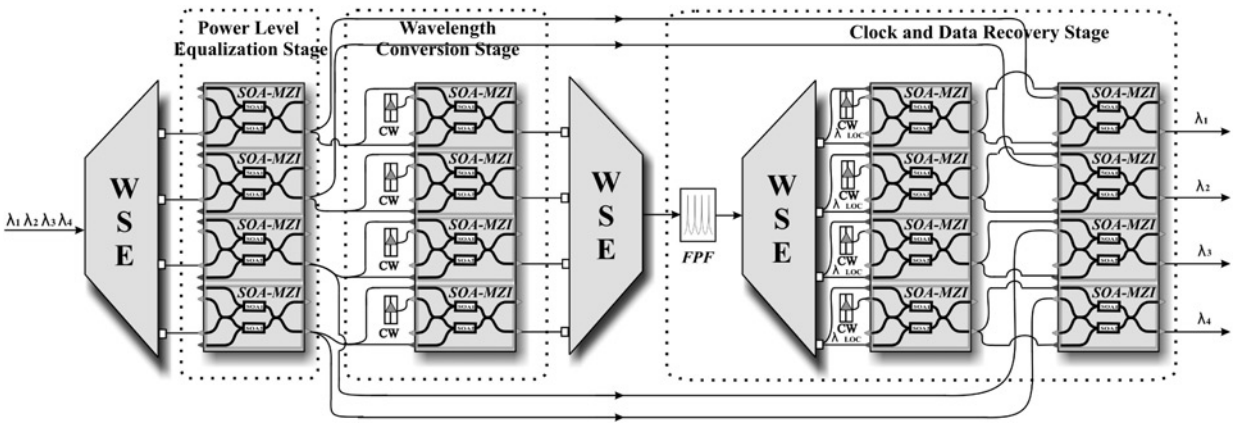

Fig. 5 *Schematic design of the four-channel burst-mode receiver using the integrated quadruple switch arrays*

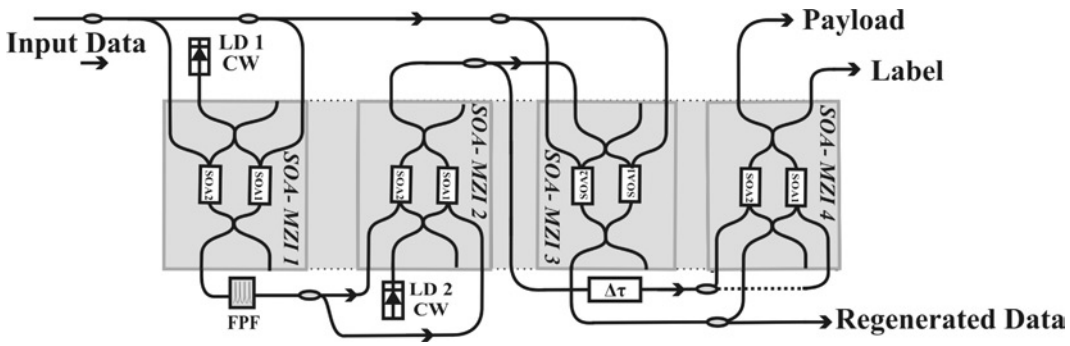

Fig. 6 *Block diagram of the whole front-end unit of an optical packet switched node based on an integrated quadruple switch array. SOA-MZI1 performs wavelength conversion, SOA-MZI2 and SOA-MZI3 are responsible for clock-and-data recovery, and HMZI4 separates the header from the payload*

each channel. Wavelength selective elements have to be employed at the input of the four-channel BMR and at both sides of the Fabry–Perot filter in order to allow for discrimination and recombination of the four wavelengths.

Although the integrated switch arrays appear as cost effective and compact solutions for a variety of WDM-processing applications, their advantages become even more pronounced in a packet-switched environment where packet-format transparency is targeted. So far, cascaded single-element SOA–MZI gates have been utilised in packet-switched configurations for the demonstration of difficult processing functionalities required in an optical packet-switched node. In this respect, the cascade of three SOA–MZI switches has been used in order to demonstrate both a header/payload separation circuit [57] as well as a short-packet 3R regenerator at 40 Gb/s [54]. In both applications, the first SOA–MZI was used as a wavelength converter and the second SOA–MZI in combination with a Fabry–Perot filter served as the packet clock recovery stage. As such, the quadruple SOA–MZI switch array could replace the discrete stages and allow for the implementation of the whole front-end unit of a packet switched node, performing wavelength conversion and packet clock recovery with two SOA–MZI gates, while the third SOA–MZI switch will be used as the decision stage for regenerating the packets and the fourth SOA–MZI will discriminate the header and the payload of the regenerated packets. The block diagram of this configuration is schematically depicted in Fig. 6.

Moreover, discrete SOA–MZI elements have been proposed as Boolean XOR comparators [58] for address recognition purposes [38] and coupled SOA–MZI switches have been demonstrated to operate successfully as optical flip-flops [59]. To this end, the use of the integrated switch array would facilitate the development of multiple XOR comparator blocks and the deployment of optical flip-flop arrays, allowing for the realisation of address recognition and buffering stages in a packet-switched node. As such, the integration of multi-element switch arrays on a single chip can certainly accommodate research efforts towards the implementation of an all-optical packet-switched node relying completely on the use of SOA–MZI gates, as envisaged within the frame of the European IST-LASAGNE project [32], by offering compactness and ease of switch interconnection.

5 Conclusion

In conclusion, we have investigated the multi-functional potential of interconnected SOA–MZI switches and have also demonstrated the first integrated quadruple SOA–MZI switch array. The multi-functionality of interconnected gates has been confirmed by means of the demonstration of the first all-optical 3R burst-mode receiver circuit, which consists of four cascaded SOA–MZI switches and is shown to receive optical bursts error-free at 40 Gb/s directly in the optical domain. In order to facilitate interconnectivity and provide compactness and ease of use, the integration of multiple switching elements on the same chip has been proposed and the first quadruple SOA–MZI switch array has been presented, constituting the first step towards photonic integration density-level increment. Quadruple SOA–MZI switch arrays can in principle allow for four-channel processing procedures like wavelength conversion and 3R regeneration in a WDM system environment, by allocating one switching element for each discriminated wavelength. Finally, we have discussed possible applications of interconnected integrated multiple-switch arrays in packet/burst-switched architectures, and have shown that integration density-level increment opens the inroad towards the development and demonstration of an all-optical high-speed packet switched node.

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