ALL-OPTICAL HALF ADDER USING TWO CASCADED UNI GATES

E. Kehayas (1), D. Tsiokos (1), K. Vyrsokinos (1), L. Stampoulidis (1), G.T. Kanellos (1), C. Bintjas (1), G. Guekos (2) and H. Avramopoulos (1)
1: Department of Electrical and Computer Engineering, National Technical University of Athens, Zographou, GR 15773, Athens, Greece
E-mail: ekeha@cc.ece.ntua.gr
2: Swiss Federal Institute of Technology Zurich, ETH Hoenggerberg, CH-8093 Zurich, Switzerland

Abstract *We present a novel all-optical half-adder using only two semiconductor interferometric gates. The first gate simultaneously performs logical AND/OR Boolean operations and the second outputs SUM and CARRY bits of 10 Gb/s pseudorandom data patterns.*

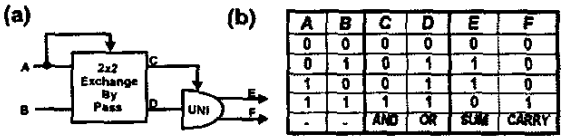
Introduction

All-optical signal processing concepts and technologies have evolved remarkably in the past few years, primarily due to the significant advancement of semiconductor-based, all-optical, switching devices [1]. One of the major practical contributions of these techniques is towards the realization of all-optical data communications, reducing o/e/o conversions in simple optical processing circuits [2], as well as optical multiprocessors and interconnects [3] for bandwidth demanding applications. Given however the complexity of all-optical switching devices, optical processing circuits must be designed to use the minimum number of optical gates achieving power efficiency and cascadability. A binary half-adder is the basic building block of a data processor performing binary addition, counting as well as data recognition and encoding [4]. Implementation of a half-adder using three all-optical TOAD gates has been shown before at 1 Gb/s [5].

In this presentation we report a simple all-optical module that uses two Ultrafast Nonlinear Interferometer (UNI) gates and operates at 10 Gb/s to perform a total of four Boolean logic operations, including that of a half-adder. The first gate is configured as a 2x2 exchange-bypass switch [6] and carries out simultaneous AND and OR logical operations. The second cascaded UNI outputs SUM (logical XOR) and CARRY (logical AND) of the original data streams hosting as the binary half-adder. Important attributes of this design are that it performs successfull Boolean operations without the need for external optical clock signals and that it is optimized in terms of active elements used.

Concept & Experimental Setup

A block diagram of the concept along with the corresponding truth table is shown in Fig. 1. The exchange-bypass switch is a 2x2 UNI-based crossbar switch, which is in the bar state when a control signal is abscent and enters cross state for the duration of the control, exchanging output ports. However, when



A	B	C	D	E	F
0	0	0	0	0	0
0	1	0	1	1	0
1	0	0	1	1	0
1	1	1	1	0	1
-	-	AND	OR	SUM	CARRY

Figure 1. (a) Concept block diagram, (b) truth table

the control signal incident on the crossbar switch is identical to one of the two incoming data streams (e.g. A), the switch outputs the logical AND and logical OR operations at ports C and D respectively. If another UNI gate is cascaded performing a simple AND between the exchange-bypass output ports, SUM and CARRY bits are generated at ports E and F respectively as shown in Fig. 1(b).

The experimental setup is shown in Fig. 2, where the three sections, namely the 10 Gb/s pseudorandom optical data pattern generator, the exchange-bypass switch (UNI1) and the UNI gate (UNI2) are clearly marked. To generate Data 1, Data 2 and Control signals, a 1545.3 nm and a 1549.2 nm DFB laser diodes (LD1, LD2) were gain switched at 1.25 GHz to produce 10 ps pulses after linear compression in dispersion compensating fiber and they were externally modulated at 1.25 Gb/s with a 2^7-1 PRBS. These patterns were passively rate multiplied using a 3-stage, fiber bit-interleaver to provide pseudorandom data patterns at 10 Gb/s.

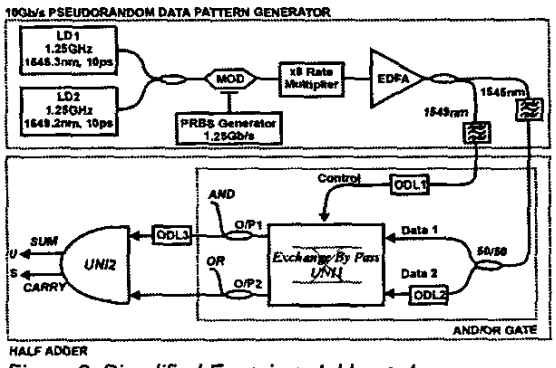


Figure 2. Simplified Experimental Layout

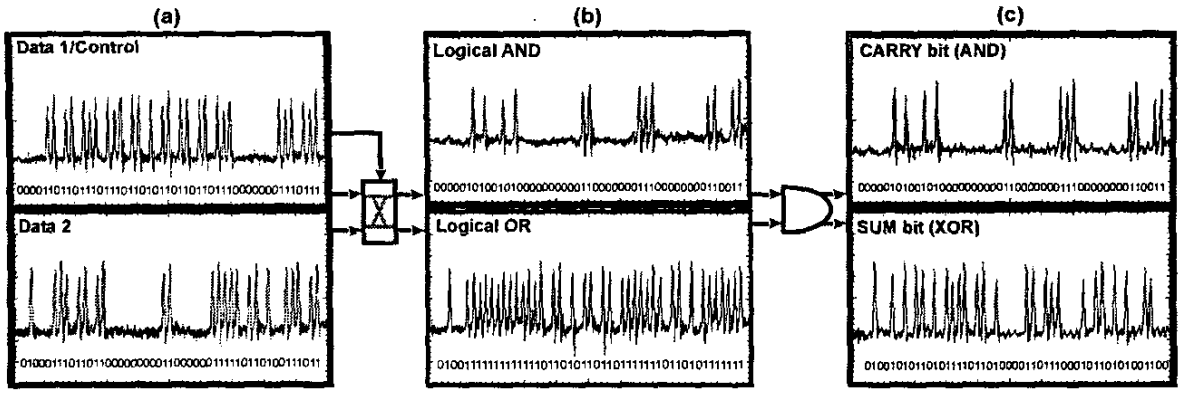


Figure 3 (a) Input data/control streams, (b) exchange-bypass outputs showing AND/OR Boolean operations (c) UNI2 gate output constituting the half adder. The time base is 500 ps/div.

The UNI-based exchange-pass switch was arranged to operate with counter-propagating signals, Data 1 and Data 2. A replica signal of Data 1 at different wavelength was used as the Control signal to allow for Data signals filtering. In this arrangement the exchange-bypass switch yields the logical AND and OR operations. The former consists of switched pulses from Data 2, while the latter consists of both Data 1 switched pulses and Data 2 unswitched pulses. The exchange-bypass [6] relies on measuring differential phase shifts between the time-separated orthogonal polarization components of the signals to be swicthed amd was optimized for 10 Gb/s operation. The non-linear switching element used was a 1.5 mm bulk SOA. Data 1, Data 2 and Control signals were bit-synchronized in the SOA using variable optical delay stages ODL1 and ODL2. To complete the half-adder circuit, a second UNI gate (UNI2) is cascaded to perform logical AND between the output of the exchange-bypass, O/P1 and O/P2, where bit synchronization was achieved with ODL3. Pulses from the OR pattern are switched in UNI2 gate whenever they coincide in time with a pulse from the AND pattern, producing the SUM bit at the Unswitched (U) port simultaneously with the CARRY bit at the Switched (S) port.

Results

Fig. 3 displays typical results of the half-adder. Fig 3(a) shows the input signals into the circuit as Data 1, Data 2 and Control. Fig. 3(b) shows the results obtained at the output of the exchange-bypass switch, verifying the logical AND and OR and fig 3(c) shows logical XOR and AND of the original data signals correspondingly as the SUM and CARRY bits of the half-adder. All logical operations were verified bit by bit and the system was tested for various data patterns. The crosstalk of the exchange-bypass switch during the bar and the cross states, was about –12 dB and –10 dB and the extinction ratio between the ON-OFF states of the UNI2 gate was approximately 8 dB. The pulse energies for operation of the exchange-bypass, (UNI1) switch were 4 fJ, 3 fJ and 9 fJ, for Data 1, Data 2 and Control signals. Similarly the pulse energies required for operation of UNI2 were 8 fJ and 2 fJ for O/P1 and O/P2 signals. These energy values are low indicating that with loss optimization of the optical circuit, signal pre-amplification between gates can be avoided.

Conclusions

We have demonstrated an all-optical half adder utilizing only two UNI gates. The logic module simultaneously perfroms AND/OR logical operations in the first stage, while SUM (logical XOR) and CARRY (logical AND) bits are generated in the second gate. Operation was tested with RZ 10Gb/s pseudorandom data patterns. The circuit design exploits the logic functionality of optical gates to perform two pairs of Boolean logic operations without requiring an external clock signal. Due to its simplicity and low pulse energies required,in principle, it can be integrated using Mach-Zehnder Interferometers [7]. Finally, since it uses only single rail logic operations, it should be capable of significantly higher speeds [8].

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