20 Gb/s Data Packet Write/Store Memory

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***Abstract**: We demonstrate a WRITE/STORE memory for 20 Gb/s data packets. The memory uses an Ultrafast Nonlinear Interferometer (UNI) and does not perform data inverting in each pass. Regenerative storage with low switching energies is verified.*

Introduction

The increasing capacity demand in fiber networks has resulted in intensified efforts to demonstrate systems capable of increasingly higher single channel line rate /1/. All-optical packet switching is a powerfull technique to provide flexible services and bandwidth consuming applications such us video-on-demand, telemedicine and Internet data transfer /2-4/. Full frames can be switched at each switch setting so as the electro-optic bottleneck at the space switches to be alleviated, however the bottleneck will apear once again at the reicever node. A key component that will help to avoid bottleneck problems in the network space switches and receiver nodes, is a robust optical memory with full write/read capability at the line rate. Regenerative memories offer the advantage over pulse-preserving one's /5/ of low jitter accumulation during storage and have been demonstrated with semiconductor optical amplifier (SOA) interferometric gates /6/. Recently a 10 Gb/s two-TOAD/SLALOM-gate memory, with wavelength conversion has been shown /7/. Also a UNI-based, all-optical circulating shift register with an inverter has also been reported, capable of storing packets of consecutive '1s' /8-9/. In this communication we report the demonstration of a single-UNI gate based regenerative memory, capable of arbitrary data packet storage at 20 Gb/s and its regeneration for many circulations. This is to our knowledge the highest-rate demonstration of arbitrary data packet storage and without data inverting on successive circulations.

Experiment

Fig. 1 shows the experimental set up which consists of a programmable optical pattern generation circuit, the UNI gate and a feedback circuit that forms the shift register. The clock signal enters the UNI, it is switched for the first time from the loading-up data sequence and consequently from the recirculating stored replicas of the sequence. The circuits are powered from two gain-switched DFB diode lasers, LD1 and LD2 that provide the clock and loading-up data packet for storage. The laser diodes were driven at 10 GHz from a signal generator and produced 9 ps pulses after fiber compression. The signal from LD2 was modulated in a $LiNbO_3$ modulator (MOD1) driven from a programmable pulse generator to produce bit sequences. The pulse trains from the diodes were bit interleaved in a split-relatively-delay-and-recombine fiber repetition rate doubler. This produced the 20 GHz clock signal and a 20 Gb/s, 32-bit long periodic data sequence of 1.56 ns duration. The clock

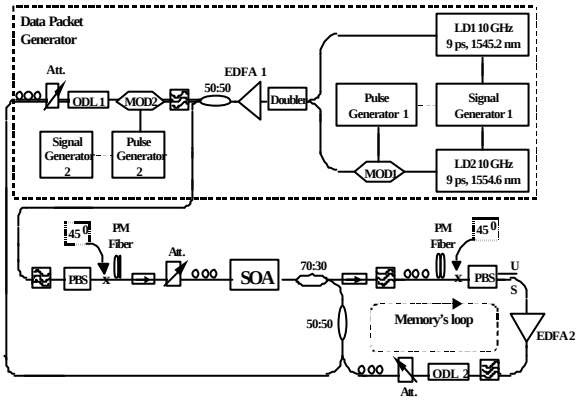

Figure 1: Experimental setup

and data sequence signals were next amplified in EDFA1 and were separated with a 3 dB coupler followed with 2 nm tunable filters. The loading-up data pattern was generated from the periodic 32-bit long sequences after transmission through a second $LiNbO_3$ modulator (MOD2), driven from pulse generator 2 operating in burst mode. Each burst mode pulse can be considered as a data packet. The number, period and width of the burst mode pulses determines the content of each data frame and can be changed at will. The total width of the frame was adjusted to correspond to the circulation time through the shift register and the period at which the frame repeats itself, defines the storage time of the frame in the memory. The 20 GHz clock signal enters the UNI through a polarization beam splitter (PBS) spliced at 45^0 to the axes of 12 m of birefringent fiber to cause 25 ps of relative delay between the fast and slow polarization components of the clock signal, before entry into the SOA.

The SOA was a 1.5 mm long bulk InGaAsP-InP ridge waveguide type SOA, with 30 dB peak small signal gain at 1561 nm when driven with 700 mA current and 80 ps recovery time. For the UNI to operate, a controlling pulse is synchronised with the relatively delayed clock polarization component to cause a differential phase change between the components. On exiting the SOA the polarization components of the clock signal were filtered and made to interfere on a PBS coupler after their relative delay was removed in birefringent fiber of equal length. The feedback circuit was completed with EDFA 2 to provide power to switch the UNI and couplers to launch the feedback signal in the SOA. The length of the feedback circuit was 77.85 m corresponding to 7785 flip-flops in the shift register. Variable delay lines ODL1 and ODL2 were used for precise time synchronisation between the three optical signals. For no controlling signal the output appears unswitched in the port U of the PBS, while otherwise it appears switched on port S. It should be noted that if there is no circuit available for loading up of the data sequence as in the majority of memory experiments, only port U may be used for the feedback, or else the memory will never start.

Results

Successful write, store and read operations were accomplished with different data packet formats over many circulations through the memory. Fig. 2a and b show

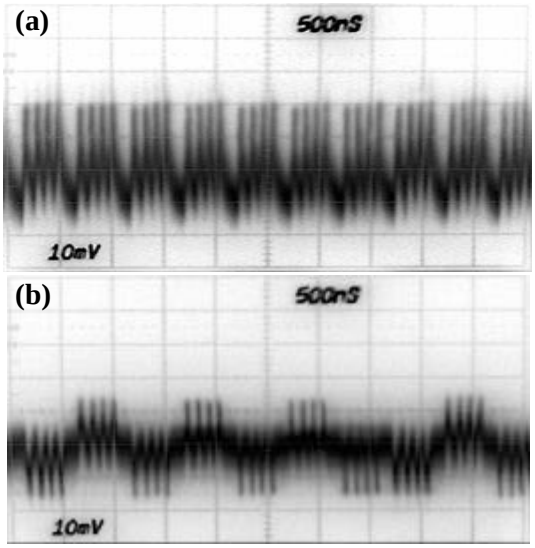

Figure 2: (a) Memory content with S-port and (b) U-port of UNI used in feedback circuit.

typical outputs with the S and U ports of the UNI feeding the memory loop monitored on a high speed analogue scope. In this instance the frame consisted of 4 data packets, each made up from 32 bit sequences and the frame is shown to recirculate for 6 times in the memory. Fig 2 shows the obvious difference in the stored signal when ports S and U are used in feedback. Port S performs straight packet storage, while port U also performs inversion in each circulation so that both the pattern and its complement appear. It is also worth pointing that the S port provides better switching and packet regeneration through the UNI and it is best used for storage purposes. In fact the stored pattern was monitored and presented no

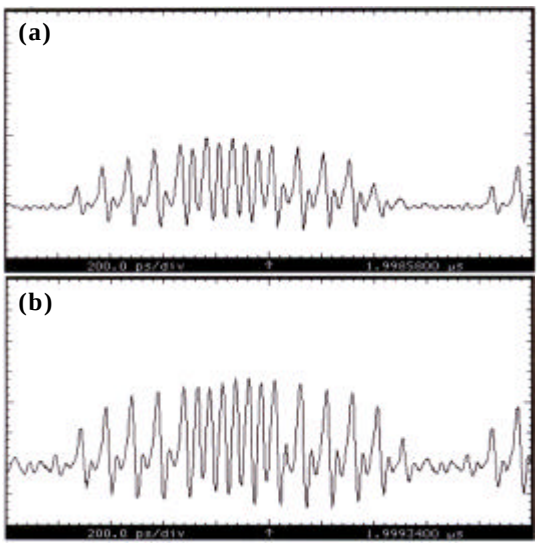

Figure 3: (a) Loading-up bit sequence and (b) pattern after 7 circulations with S-port in feedback. The time base is 200 ps.

deterioration for more than 42 circulations through the memory corresponding to more than 21 μs storage time. This number of recirculations through the memory does not represent its long-term storage limit, but is rather imposed by limitations of our diagnostic instrumentation.
The quality of the stored patterns were also investigated with a 40 GHz sampling scope. Fig 3(a) and (b) show the loading-up pattern before storage and the stored pattern after 7 circulations, indicating improvement in the contrast of the stored bits. The slow modulation that appears on both the initial and stored patterns is due to the electrical pulse driving the modulator MOD1. The pules energies of the clock, loading up signal and recirculating signal was 3 fJ, 23 fJ and 33 fJ respectively, making this memory a low energy consumption circuit.

Conclusions

In conclusion we have demonstrated an all-optical, writeable and regenerative loop memory operating with 20 Gb/s data packets of variable length and spacing and low energy to perfrom. Data packet regeneration has been verified for more than 42 times.

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