All-optical Write/Read Memory for 20 Gb/s Data Packets

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We demonstrate a writeable all-optical memory for variable length, 20 Gb/s data packets. The memory uses an Ultrafast Nonlinear Interferometer (UNI) gate and does not perform data inverting in each pass. Regenerative storage with low switching energies is verified.

Introduction: In recent years the ever increasing capacity demands in optical fiber networks has spurned efforts towards higher single channel line rates [1] and all-optical signal processing systems [2-4]. One essential subsystem that will help in the realisation of high capacity, optical packet switched networks, is a robust optical memory with full write/read capability at the line rate. Regenerative memories using optical fiber as the shift register and all-optical gates for regeneration [5] offer the advantage of low jitter accumulation during storage. Semiconductor optical amplifier (SOA) interferometric gates have been used increasingly, because of their low switching energies and latencies [6]. A UNI-based, all-optical circulating shift register with an inverter has been reported, capable of storing packets of consecutive '1s' at 40 Gb/s [7] and more recently a UNI-based regenerative memory has been demonstrated, capable of storing 10 Gb/s of data error-free [8]. In this communication we report the demonstration of a single-UNI gate regenerative memory, capable of arbitrary data packet storage at 20 Gb/s and its regeneration for many circulations. This is

to our knowledge the highest-rate demonstration of arbitrary data packet storage and without data inverting on successive circulations.

Experiment: Fig. 1 shows the experimental set up which consists of a programmable optical pattern generation circuit, the UNI gate and a feedback circuit that forms the shift register. The clock signal enters the UNI, it is switched for the first time from the loading-up data sequence and consequently it is switched from the recirculating stored replicas of the sequence. The circuits are powered from two gain-switched DFB diode lasers, LD1 and LD2 that provide the clock and loading-up data packet for storage. The laser diodes were driven at 10 GHz from a signal generator and produced 9 ps pulses after fiber compression. The signal from LD2 was modulated in a $LiNbO_3$ modulator (MOD1) driven from a programmable pulse generator to produce bit sequences. The pulse trains from the diodes were bit interleaved in a split-relatively-delay-and-recombine fiber repetition rate doubler. This produced the 20 GHz clock signal and a 20 Gb/s, 32-bit long periodic data sequence of 1.56 ns duration. The clock and data sequence signals were next amplified in EDFA1 and were separated with a 3 dB coupler followed with 2 nm tunable filters. The loading-up data pattern was generated from the periodic 32-bit long sequences after transmission through a second $LiNbO_3$ modulator (MOD2), driven from pulse generator 2 operating in burst mode. Each burst mode pulse can be considered as a data packet. The number, period and width of the burst mode pulses determines the content of each data frame and can be changed at will. The total width of the frame was adjusted to correspond to the circulation time through the shift register and the period at which the frame repeats itself, determines the number of

recirculations or storage time of the frame in the memory. The 20 GHz clock signal enters the UNI through a polarization beam splitter (PBS) spliced at 45^0 to the axes of 12 m of birefringent fiber to cause 25 ps of relative delay between the fast and slow polarization components of the clock signal, before entry into the SOA. The SOA was a 1.5 mm long bulk InGaAsP-InP ridge waveguide type device, with 30 dB peak small signal gain at 1561 nm when driven with 700 mA current and about 80 ps recovery time. For the UNI to operate, a controlling pulse is synchronized with the relatively delayed clock polarization component to cause a differential phase change between the components. On exiting the SOA the polarization components of the clock signal were filtered and made to interfere on a PBS coupler after their relative delay was removed in a birefringent fiber of equal length. The feedback circuit was completed with EDFA 2 to provide power to switch the UNI and couplers to launch the feedback signal in the SOA. The length of the feedback circuit was 77.85 m corresponding to 7785 flip-flops in the shift register. Variable delay lines ODL1 and ODL2 were used for precise time synchronization between the three optical signals. For no controlling signal the output appears unswitched in the port U of the PBS, while otherwise it appears switched on port S.It should be noted that if there is no circuit available for loading up of the data sequence as in the majority of memory experiments, only port U may be used for the feedback, or else the memory will never start.

Results: Successful write, store and read operations were accomplished with different data packet formats over many circulations through the memory. Fig. 2a and b show the outputs of typical stored patterns using the switched port S of

the UNI for feedback of the memory loop. The frames consisted of 2 data packets in fig 2(a) and 4 packets in fig 2(b), while each packet was made out of 32 bit sequences. Fig 2 also shows that the use of the S-port of the UNI causes no data inverting [7] during the 7 times recirculation through the memory. It was possible to monitor the stored pattern through more than 42 successive circulations, corresponding to more than 21 μs of storage time and the stored pattern still presented no deterioration. It should be noted that this number of recirculations is not the long-term-time storage limit of the memory, but is rather imposed by limitations of our diagnostic instrumentation. It was also possible to use the unswitched port U of the UNI for storage. However switching through the U-port is not so good and the regenerative ability of the memory is impaired. Fig. 3 (a), (b) and (c) show the loading-up pattern before storage, the stored pattern with the S and U-ports respectively after 7 circulations on a 40 GHz sampling scope. Fig 3 shows that the performance of the memory using the S-port for feedback is far superior due to the better switching of this port. The slow modulation that appears on the patterns is due to the electrical pulse driving the modulator MOD1. The pulse energies of the clock, loading up signal and recirculating signal was 3 fJ, 23 fJ and 33 fJ respectively, making this memory a low energy consumption circuit.

Conclusions: In conclusion we have demonstrated an all-optical, writeable and regenerative loop memory operating with 20 Gb/s data packets of variable format and low energy to operate. Data packet regeneration has been verified for more than 42 times.

References

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Figure captions:

Fig.1 Experimental setup.

Fig.2 (a) and (b) Memory content with S-port of UNI used in feedback circuit for different packets.

Fig.3 (a) Loading-up bit sequence and pattern after 7 circulations using (b) S-port and (c) U-port in feedback.The time base is 200 ps.

Figure 1

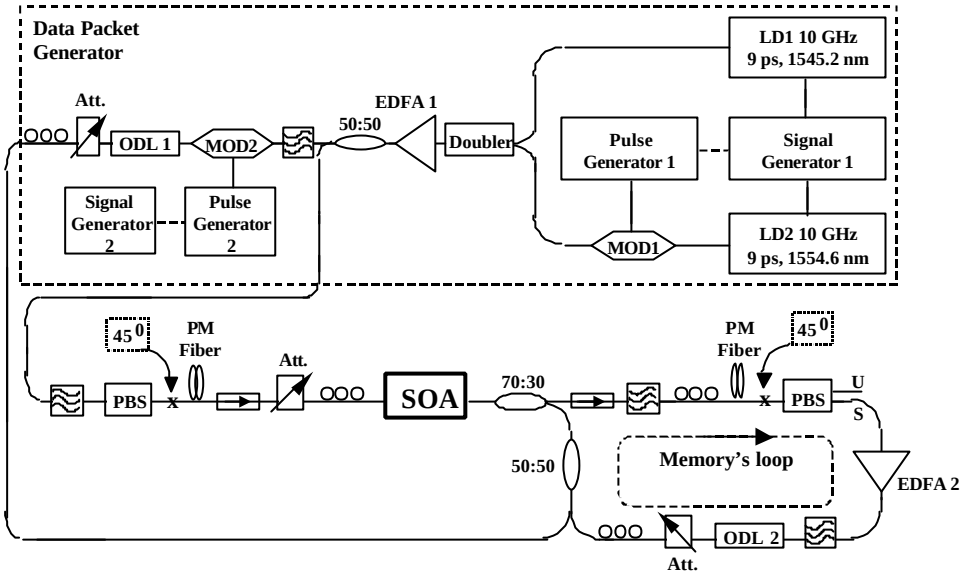

Data Packet Generator
LD1 10 GHz 9 ps, 1545.2 nm
Att.
EDFA 1
50:50
ODL 1
MOD2
Doubler
Pulse Generator 1
Signal Generator 1
Signal Generator 2
Pulse Generator 2
MOD1
LD2 10 GHz 9 ps, 1554.6 nm
45 0
PM Fiber
Att.
PM Fiber
45 0
PBS
SOA
70:30
PBS
U
S
50:50
Memory's loop
EDFA 2
ODL 2
Att.

Figure 2

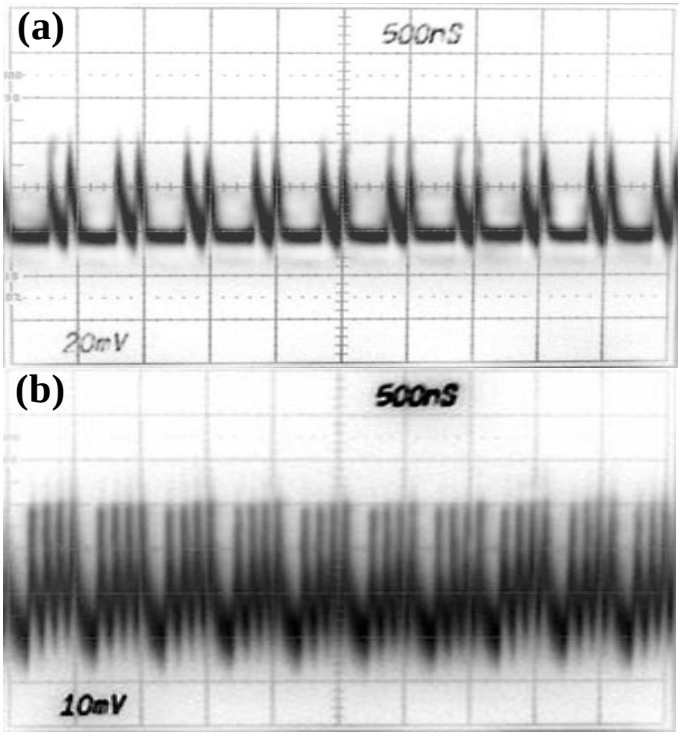
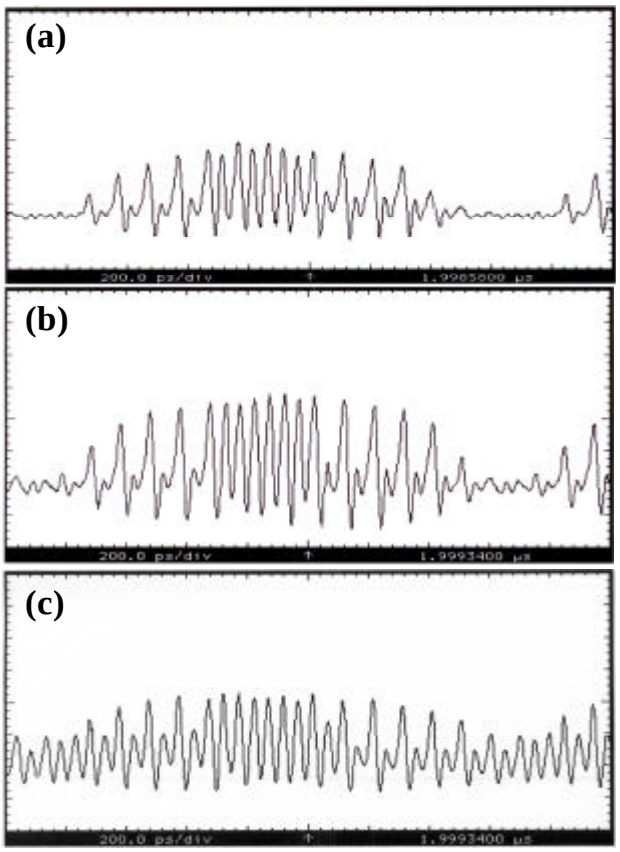


Figure 3


(a)
200.0 ps/div
1.9985000 µs
(b)
200.0 ps/div
1.9993400 µs
(c)
200.0 ps/div
1.9993400 µs