New generation integrated photonic systems-on-chip enabling Tb/s-capacity Photonic Routers

(Invited)

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Abstract
We present recent advances in functional photonic integration and its application for the realization of photonic Tb/s routing. Specifically, we report on the transition from single element to multi-element photonic devices with the fabrication of the first hybrid integrated arrays of optical switches using the silica on-silicon hybrid photonic integration technique. We demonstrate how the enhanced processing power of these components can be exploited to implement key functionalities required in next generation, fully integrated, Tb/s photonic routers.
Keywords: photonic routers, optical packet switching, all-optical wavelength converters, photonic integration, silicon optical bench, functional integration

1. Introduction

The potential of photonic routing as a solution for the capacity scaling of electronic routers is the driver for intensive research efforts and investment worldwide. The role of optics in high-capacity routing has been thoroughly examined and experts are claiming that optical technologies show an excellent potential for inclusion in high capacity routers [1]. Now the focus is on photonic integration and the development of components with high integration density, intelligence and capability to deliver the functionalities of a photonic router - the “machine” that will take over the switching and routing of data, promising low power consumption and footprint. The pieces of the puzzle are being gathered with the demonstration of the first photonic systems-on-chip: indium phosphide (InP) chips that perform packet forwarding [2], packet envelope detection (PED) [3] and wavelength switching [4], as well as integrated buffers [5] and integrated Arrayed Waveguide Grating (AWG) switching fabrics [6]. The moving target is to integrate more and more optical processing elements into the same chip in order to bring down cost, which is dominated by the use of discrete devices. A photonic integration platform, which will allow higher levels of flexible, functional and cost-effective integration, is expected to lead to the development of compact, high-speed “optical line cards” and thus open the possibility for scalable and fully integrated Tb/s photonic routers.

The silica-on-silicon hybrid integration developed by the Center for Integrated Photonics (CIP UK) is a technique that enables flip-chip bonding of pre-fabricated InP components, including SOAs and modulators on silicon boards with low loss waveguides [7]. The approach has been successfully used for the development of single element, all-optical wavelength converters and due to the passive assembly process it shows great potential for the development of advanced photonic components. Seeking for a scalable solution for wavelength conversion (required for the wavelength routing process in a photonic router), we recently managed to expand the silica-on-silicon system and report the first quadruple arrays of 40 Gb/s wavelength converters. The integration of multiple switching elements on the same silicon chip, reduces packaging and pigtailing costs while increases the integration density level. Application-wise, we present the benefits gained from such an expansion: apart from the obvious advantage of having a single-chip, WDM wavelength conversion stage, the multi-element components can be used to realize the most demanding functionalities including PED-based contention resolution, label/payload separation, clock recovery and 3R regeneration. The first step for the transition from single element to multi-element hybrid integrated photonic devices has been made.

2. Hybrid integrated arrays of SOA-MZI switches

The hybrid integration technology relies on the unique combination of high-speed InP monolithic elements, precision-machined silicon (Si) submounts and low-loss silica-on-silicon planar lightwave circuits (PLC) for achieving characteristics such as high yield, small footprint, device scaling and low power consumption. A planar silica-on-silicon waveguide platform acts as a motherboard to host both active and passive devices. Integration is achieved by using precision-machined silicon submounts or “daughterboards” carrying individual optical components into the motherboard. The individual components have precision cleaved features for accurate mechanical positioning on the daughterboard. For the quad array device, two monolithic arrays of precision-cleaved SOAs are mounted on two micromachined silicon submounts, by pushing the monolithic chip against end stops on the submount and reflowing solder. Apart from the passive waveguide network, the motherboard employs the mechanical end stops and landing site features to enable the passive, flip-chip assembly of the two daughterboards. Figure 1 shows a packaged and pigtailed single and quadruple array of SOA-MZIs, whereas Table 1 summarizes the specifications of both devices, showing in numbers the advancements achieved by the expansion of the hybrid photonic platform. The quad array device with 160 Gb/s aggregate chip throughput (4 times higher than the single element) hosts 8 SOAs and 8 phase shifters in a slightly increased chip area. It is evident that the reduction of packaging and pigtailing costs comes with a significant increase in chip processing capability while consuming the same board space.

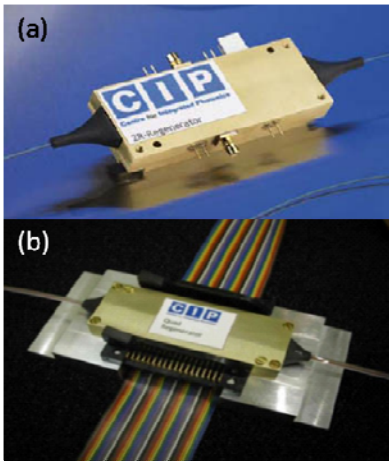

Table 1. Brief benchmarking of single and quad array SOA-MZI switches

Parameter / Device	Single SOA-MZI	Quad SOA-MZI array
Chip throughput	40 Gb/s	160 Gb/s (4x40 Gb/s)
number of SOAs	2	8
number of phase shifters	2	8
Chip size (motherboard) (W)x(L)	11 mm x 44 mm	15 mm x 58 mm
Total size of device (L)x(W)x(D)	72 mm x 30 mm x14 mm	90 mm x 32 mm x 12 mm

Figure 1. Single (a) and quad (b) device

3. Applications

3.1 Multi-channel wavelength conversion

The first milestone that has been set to prove the reliability and multi-functionality of the integrated arrays of SOA-MZI switches is to prove that the technique can be employed to implement a scalable and compact wavelength routing stage of a photonic router. This means the demonstration of multi-channel wavelength conversion required for the routing of optical packets through the AWGR as well as for multi-casting purposes. Four CW lasers (wavelengths 1554, 1556, 1558 and 1559 nm) have been used to power each one of the four wavelength converters of the quad device and convert the wavelength of a 10Gb/s NRZ packet stream. Figure 2a) shows the eye diagrams of the incoming packet-mode (left column) and wavelength converted (right column) signals. Figure 2b) depicts bit-error-rate curves that were obtained for the input and output signals. The circuit performed error-free for all four outputs with a maximum power penalty of 1.68 dB.

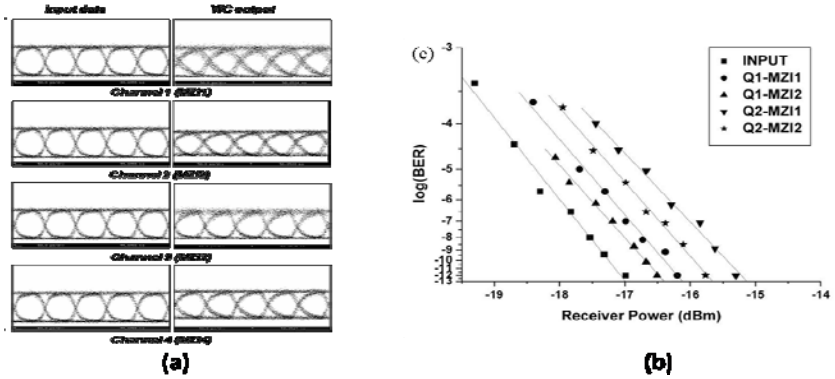

Figure 2. Experimental results for multi-channel wavelength conversion

3.2 On-the-fly, packet-mode, all-optical contention resolution

In this section we present an all-optical sub-system performing on-the-fly contention resolution implemented with the hybrid integrated SOA-MZI gates. The sub-system is capable of operating for both Non-Return and Return-to-Zero (NRZ and RZ)

modulation formats by utilizing an all-optical packet envelope detection circuit and additional optical gates for performing deflection and wavelength conversion of contending packets. Figure 3a) shows the schematic diagram of the optical system that is capable of resolving contention for two incoming packet streams that are on the same wavelength (λ1). The circuit has two input ports and a single output port and employs packet detection, optical space switching and wavelength conversion. The PED circuit consists of a passive filter in combination with a SOA-MZI optical gate operated as a low-bandwidth 2R regenerator.

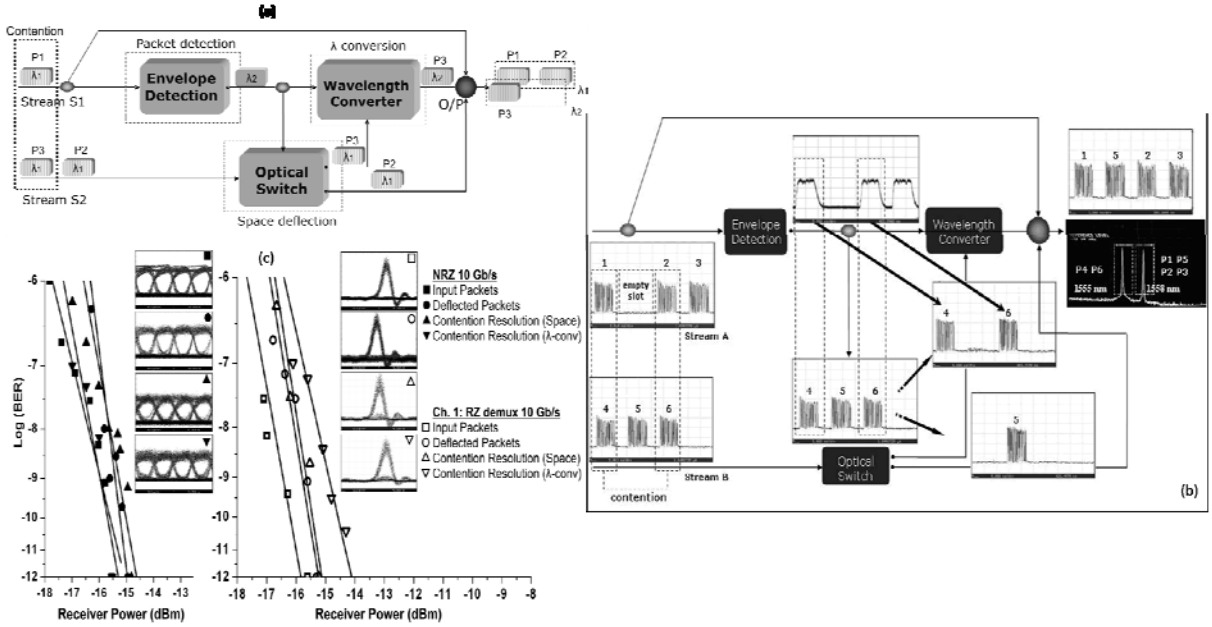

Figure 3. Concept (a) and experimental results (b-c) for all-optical contention resolution.

The PED circuit generates a packet envelope, indicating the presence of a packet at the specific timeslot (P1 in Figure 3a). Contention resolution in space is achieved by triggering the 1x2 switch with the PED signals generated by stream S1 to control packet stream S2. As such, the packets of stream S2 are spatially separated (switched) at the 1x2 optical switch. The contenting part of this packet stream can either enter a recirculating buffer or be deflected to a different output port or be wavelength converted, depending on the contention resolution strategy and the architecture of the router. In this case, we demonstrate contention resolution in the wavelength domain, using the same PED signal to wavelength convert the deflected packets. Hence, the packets of stream S2 contending with the packets of stream S1 are wavelength converted onto the packet envelope (λ2) generated by stream S1. Figure 3b) shows time-domain results for contention resolution of 10 Gb/s NRZ optical packets. Two cases of contention between streams A and B are indicated as well as the presence of an empty slot in stream A. Stream A is launched in the PED circuit which extracts the envelopes of packets 1, 2 and 3. When Stream B reaches the 1x2 switch, it is triggered by the PED signal so that packets 4 and 6 appear at the switched port, whereas packet 5 is spatially separated. Packet 5 is directly forwarded to the output together with stream A and fills the empty slot after combination of the two signals in a passive coupler. As a result, a time multiplexed packet stream consisting of packets 1, 5, 2 and 3 appears at the output, whereas packets 4 and

6 are wavelength converted by the PEDs and forwarded through the third port of the coupler avoiding any collision. The Optical Spectrum Analyzer (OSA) trace indicates the presence of two wavelengths at the output of the system, namely 1558nm for packets 1, 5, 2 and 3 and 1555nm for packets 4 and 6. Figure 3c) shows the BER curves obtained for the deflected, time multiplexed and wavelength converted packets for both 10 Gb/s NRZ and 40 Gb/s RZ operation. The power penalties are less than 1 dB in the case of 10 Gb/s operation and less than 2 dB at 40 Gb/s.

3.3 High-speed, all-optical wavelength conversion, label recovery and data regeneration

Apart from a scalable solution for multi-channel wavelength conversion, the hybrid integrated switch arrays present a unique opportunity for multi-functionality, i.e. simultaneous performance of functionalities using multi-signal processing on a single chip. Here we demonstrate the processing power and multi-functionality of the quadruple array device by performing wavelength conversion, clock recovery, data regeneration and label/payload separation using a single photonic integrated chip. Each SOA-MZI switch of the array is assigned a different role operating as: wavelength converter, amplitude equalizer in the clock recovery unit, regenerator and AND gate for label/payload separation (fig. 4a)). After the wavelength conversion process, the signal is fed into the clock recovery circuit which employs a low-Q Fiber Fabry Perot filter and a SOA-MZI gate as equalizer. The recovered clock has a double role: 1) it is used as the input signal to the 3R decision gate, where retiming and reshaping is achieved by triggering the incoming data with the retimed optical recovered clock pulses and 2) it is delayed and used to perform an AND operation with the incoming data to perform label recovery. Figure 4b) and c) show the time-domain results recorded after EAM-based demultiplexing, as well as the BER measurements. The BER measurements reveal a negative power penalty of up to -1.9 dB for the regenerated data. Negative power penalties of -0.7 and -0.2 dB were also measured for the extracted payload and label channels respectively with respect to the input data.

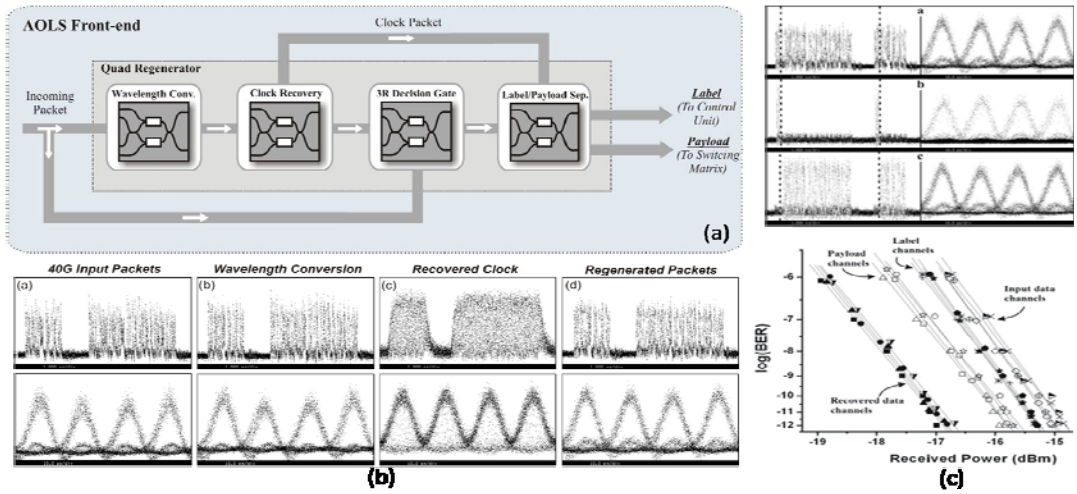

Figure 4. Concept (a) and experimental results (b-c) for label recovery and 3R regeneration.

4. Conclusion

We have described recent advances in multi-element photonic integration and specifically the development of the first hybrid integrated arrays of high-speed, wavelength converters. The devices have been used to demonstrate almost all the functionalities required in a high-capacity photonic router including multi-channel wavelength conversion, packet-envelope detection, label recovery, contention resolution and data regeneration.

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References

[1] R. S. Tucker," The Role of Optics and Electronics in High-Capacity Routers", *J. Lightwave Technol.*, vol 26, no12, Dec 2006, pp. 4655-4673.

[2] V. Lal,et al, "Monolithic Wavelength Converters for High-Speed Packet-Switched Optical Networks", *J. Selected Topics in Quantum Electronics*, Vol. 13, Issue 1, Jan.-Feb. 2007 pp. 49-57.

[3] B. R. Koch, et al, "Payload-Envelope Detection and Label-Detection Integrated Photonic Circuit for Asynchronous Variable-Length Optical-Packet Switching With 40-Gb/s RZ Payloads and 10-Gb/s NRZ Labels,", *J. Lightwave Technol.*, Vol. 24, No. 9, pp. 3409-3417, Sept. 2006

[4] P. Bernasconi, W. Yang, L. Zhang, N. Sauer, L. Buhl, I. Kang, S. Chandrasekhar, D. Neilson, "Monolithically Integrated 40Gb/s Wavelength Converter with Multi-Frequency Laser," *in Proc. OFC 2005*, Anaheim, CA, March 7-11,2005, PDP16.

[5] E.F. Burmeister, J.E. Bowers, Integrated gate matrix switch for optical packet buffering, *IEEE Photon. Technol. Lett.*, 18 (1), (2006) 103–105.

[6] Jürgen Gripp, "The IRIS Optical Packet Router: A DARPA / MTO Project", International Workshop on the Future of Optical Networking (FON), *OFC 2006*, Anaheim, USA.

[7] G. Maxwell, "Low-cost hybrid photonic integrated circuits using passive alignment techniques", invited paper MJ2, *IEEE-LEOS Annual Meeting*, Montreal, Canada (2006).