A Hybrid Photonic Integrated Wavelength Converter on a Silicon-on-Insulator Substrate

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Abstract: We present fabrication and testing of a wavelength converter integrated on a silicon-on-insulator substrate. The chip employs a hybrid integrated SOA and delay-interferometers integrated on 4µm SOI. We demonstrate 40Gb/s error-free performance.
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1. Introduction

Hybrid integration on silicon substrates is attempted as a practical solution to generate compact, high-performance photonic integrated circuits (PICs). Silicon-on-insulator (SOI) - as an integration board - is attractive due to the cost-effective material and versatility; SOI substrates can be engineered to permit diverse single mode waveguide dimensions from hundreds of nanometers (nanowires) to tens of micrometers (rib waveguides). In the case of silicon nanowires, die-to-wafer bonding has enabled the integration of a variety of active components including micro-disk lasers [1] and photodetectors [2]. This technique has lead to commercial devices for optical interconnects and data communications. The application range of "hybrid silicon photonics" can be expanded with the utilization of integration boards with micro-meter scale dimensions. This waveguide technology enables the hybridization of mature, pre-fabricated III-V components due to the excellent matching of the optical modes between active chips and silicon rib waveguides. Flip-chip mounting methods based on thermo-compression are being developed for fabricating fully integrated and packaged hybrid silicon devices incorporating III-V lasers, photodetctors, high-speed modulators or semiconductor optical amplifiers (SOAs) [3-4]. Another type of hybrid integration based on micro-solder bumps is now being attempted for the fabrication of all-optical wavelength converters (AOWCs) [5] applicable to next generation wavelength routed core networks.

In this paper we demonstrate the fabrication and experimental testing of an all-optical wavelength converter hybrid integrated on a 4 µm SOI rib waveguide substrate. The photonic chip incorporates a 1.25 mm prefabricated non-linear SOA mounted on the SOI board using gold-tin bumps as small as 14 um and with lateral placement misalignment <1um. Optical filtering is realized by two cascaded delay interferometers (DIs) integrated on the SOI board using 2x2 multi-mode interference (MMI) couplers. Full free spectral range (FSR) tuning of the DIs is accomplished by two independently tuned on-chip thermal heaters. We demonstrate 40 Gb/s error-free wavelength conversion (WC) with power penalties < 4 dB and power consumption of only 700mW.

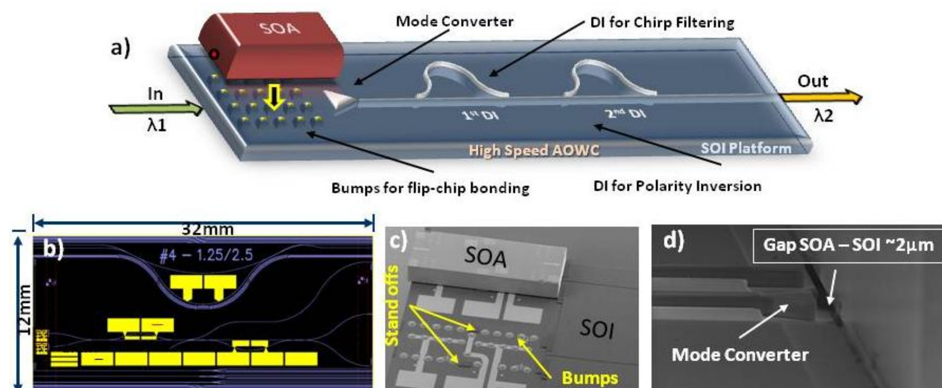

Figure 1: a) Layout of hybrid AOWC, b) Mask design, c) SEM image of SOA bonded on SOI, d) SEM of SOA and SOI taper section

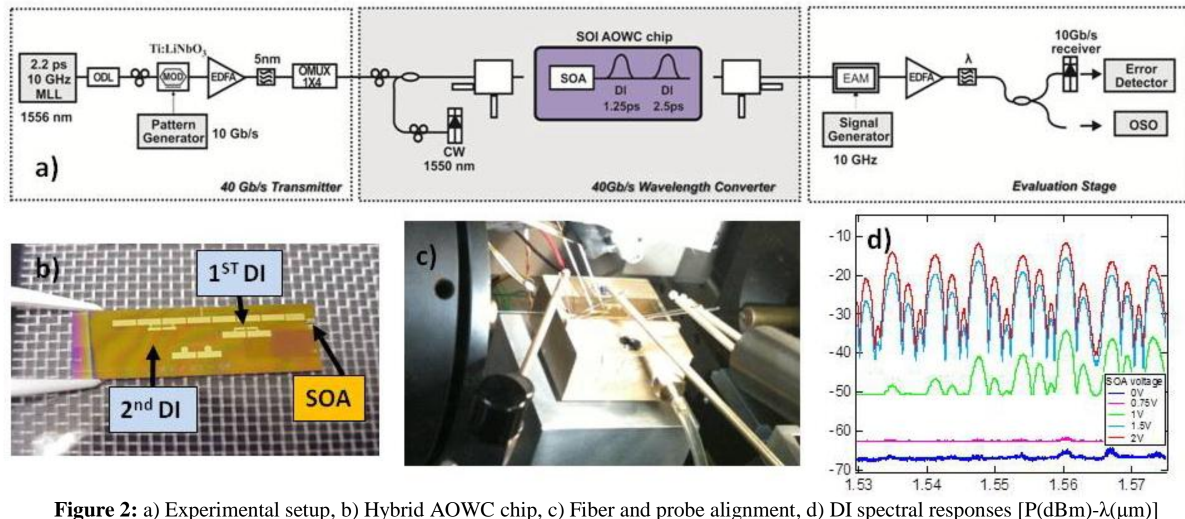

Figure 2: a) Experimental setup, b) Hybrid AOWC chip, c) Fiber and probe alignment, d) DI spectral responses [P(dBm)-λ(μm)]

2. Concept, Fabrication and Experimental Setup

Figure 1a) depicts the layout of the hybrid SOI AOWC. The whole structure features two basic components : the SOA and the SOI integration board. The SOA is used as non linear element for wavelength conversion by means of cross gain and cross phase modulation effects. The SOI integration board on the other hand performs add-on wavelength processing with two cascaded delay interferometers. The first one is utilized as periodic WDM filter for chirp filtering and SOA recovery time acceleration, whereas the second one as filter notch for polarity inversion. Both SOA and SOI functionalities are combined in the same platform under the following procedure. A part of the SOI platform undergoes processing and bump deposition forming a reception area for a SOA which is flip-chip bonded on the SOI substrate, aligned to the SOI waveguide and mode matched through a tapered section.

Fabrication procedure starts first with the generation of 1.25mm flip-chip mounted SOAs. For the current flip-chip adapted SOA design, a buried heterostructure with pn current blocking layers has been employed incorporating laterally tapered input/output waveguides serving as spot-size converters. For alignment, dry etched trenches have been implemented in the backside of the chip acting as counterparts to the reception motherboard stand-offs. Regarding the SOI board fabrication three individual steps have been followed: a) SOI waveguide etch and integration zone processing (etch through buried oxide and etch of alignment stands), b) complete metallization of SOI motherboard with electrical interconnects, Under Bumb Metallization (UBM) and AuSn bump sputtering and c) back-end preparation of singled out motherboard dies with inspection and facet polishing. With respect to the flip-chip mounting of the SOA into the SOI substrate, this has been performed by a high accuracy flip-chip bonder that undertakes the positioning against the stand-offs and the thermal cycling for bump reflow and soldering. The reproducibility/uniformity of bump ball fabrication and the lift off the required post processing (optimized reflow and soldering) has been achieved after a a series of trial tests resulting to devices with proper mechanical stability and contact quality. Figure 1b) depicts the developed SOI board mask layout with the SOA integration zone, the cascaded DIs and the heating elements. Figure 1c) shows in turn a close view of the SOI integration zone after bump deposition and metallization as well as the flip-chip bonded SOA on the SOI motherboard. Finally figure 1d) presents the good horizontal and vertical alignment of the SOA facet with the SOI waveguide.

Figure 2a) illustrates the experimental setup used for the system testing of the hybrid AOWC. The 40Gb/s transmitter was generated by time interleaving the 2.2ps output of a 10 GHz mode-locked laser modulated with a 2^7-1 PRBS. For the wavelength conversion part, the 40G data source at 1556nm and the signal from a DFB laser at 1550nm were combined and coupled into the hybrid silicon chip for cross gain-phase modulation, chirp filtering and polarity inversion. The output of the AOWC was evaluated with BER measurements after performing demultiplexing to 10Gb/s using an Electro-Absorption Modulator (EAM). Figure 2b) shows the fabricated hybrid AOWC with the SOA bonded on the SOI board while figure 2c) the sample placed on the alignment station with 6 probe tips on top for SOA driving and DI wavelength tuning. Figure 2d) depicts in turn the extracted AOWC filter characteristics at SOA currents from 0-200 mA using a tunable laser as seed with 8dBm output power.

3. Results and Discussion

Figure 3a) shows the incoming 40G data stream which was injected into the SOA for cross gain and phase modulation. Figure 3b) illustrates the inverted wavelength converted signal when detuning the DI filter

characteristics 0.3nm off the signal carrier for effective chirp filtering and recovery acceleration. Figure 3c) depicts the non-inverted wavelength converted signal when placing the carrier in a filter notch generated by tuning and overlapping two subsequent DI filter dips. With a total power of 40mW in the integrated heating elements, a response with ~30 dB extinction was obtained for sufficient spectral carrier suppression. Although the signal polarity was effectively restored, the low output power measured at the output of the AOWC resulted to an amplified waveform with low OSNR and amplitude noise.

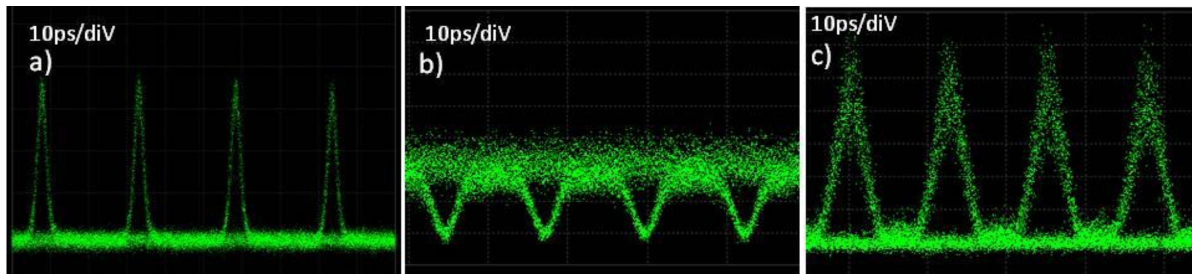

Figure 3: Eye-diagrams of a) B2B signal, b) Inverted signal after AOWC, c) Non-inverted signal after AOWC

Figure 4a) depicts the BER curves of the back-to-back and non-inverted WC. Error-free operation was achieved for all the demultiplexed channels with power penalties less than 4dB. The high penalty was attributed to the low power and bad quality signal after spectral carrier suppression and amplification respectively. SEM inspection in the chip has revealed that a 3 µm lateral misalignment between the SOA facet and SOI waveguide was responsible for the high insertion loss observed. Next generation hybrid AOWCs are expected to have higher optical power improving wavelength conversion performance significantly. Figure 4 b) shows the spectral output obtained after cross gain and phase modulation while figure 4c) the non-inverted spectrum after carrier suppression.

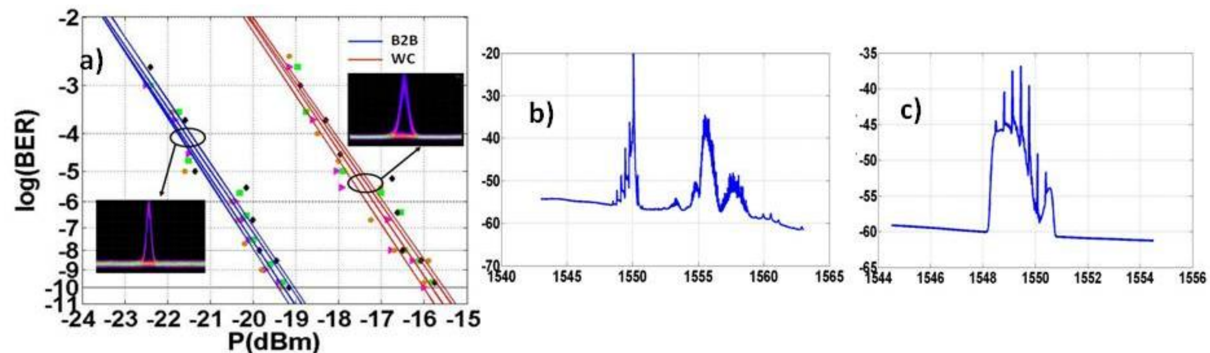

Figure 4: a) BER of B2B and Non-Inv WC, b) Spectral output after inverted WC, c) Non-Inverted spectrum [P(dBm)-λ(nm)]

4. Conclusions

We have fabricated and system tested a hybrid all-optical wavelength converter on a silicon-on-insulator substrate. The photonic chip consumes 700mW and performs inverted and non-inverted wavelength conversion using a flip-chip mounted SOA and two concatenated delay interferometers. Error-free operation has been accomplished at 40Gb/s with power penalty less than 4dB.

5. References

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