480 Gb/s WDM (12×40 Gb/s) data transmission over a dielectric-loaded plasmonic waveguide

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Abstract: We demonstrate 480 Gb/s (12×40 Gb/s) WDM enabled data transmission through a dielectric loaded plasmonic waveguide. Error-free performance with power penalties ranging between 0.2-1 dB has been obtained for six out of the twelve channels.
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1. Introduction

The rapid advances witnessed during the last decade in the field of plasmonics have been accompanied by a great promise for reducing power consumption and increasing integration densities in optical interconnects, with Surface Plasmon Polaritons (SPPs) being heralded as the next-generation chip-scale data information carriers [1]. These expectations have been stimulated by the inherent SPP wave propagation principles and have been further strengthened by the remarkable progress in plasmonic waveguide and device technologies. SPPs are travelling along metal circuitry offering strong mode confinement and a "natural" interface for the power-efficient interaction between light beams and electronic control signals. Among the various plasmonic waveguide structures proposed so far, the seamless light-electron interactive mechanism has been mainly highlighted in the case of Dielectric-Loaded SPP waveguides (DLSPPW), which employ a dielectric polymer material on top of the metallic film. Their potential to yield low-footprint, highly functional and low-power on-chip circuitry for interconnect purposes has been demonstrated in recent preliminary experimental and theoretical studies [2-4] on the thermo-optic tuning of Polymethylmethacrylate (PMMA)-loaded SPP structures and on their use for power monitoring purposes [5].

However, DLSPPW performance has never been addressed with respect to Tbps-scale Wavelength Division Multiplexed (WDM) transmission metrics required by real interconnect systems, still lacking a solid evidence of their system-qualified application perspectives in data traffic conditions that usually apply to photonic Network-on-Chip (NoC) solutions for future optical interconnect systems [6]. The main reason for this has been the high propagation loss of the DLSPP platform that has hindered its communication with the outer world photonic elements. Efforts towards counteracting the loss-associated problems have concentrated on their interconnection to lower-loss waveguide platforms [7,8] still not concluding however to a solid proof of their data transfer capabilities in real Tb/s WDM chip-scale interconnects. So far, only Long-Range SPP (LRSPP) waveguides have been experimentally proven to serve as data transmission lines up to 40 Gb/s line rates [9], but LRSPPs have significantly weaker mode confinement and a restricted functional quiver, negating the circuit size and power consumption advantages envisioned by the introduction of plasmonics. The DLSPPW platform has been only recently addressed with respect to its single-channel signal integrity and data carrying properties exploiting the integration of PMMA-loaded SPP structures on a Silicon-on-Insulator (SOI) platform [2], showing successful performance in 10 Gb/s line-rate transmission.

In the present communication, we report on WDM-enabled transmission of 0.48 Tb/s aggregate traffic (12×40 Gb/s) through a straight DLSPPW. The DLSPP-on-SOI chip reported in [2] was exploited to allow for the in- and out-coupling of the WDM signal and its introduction into a 60-μm-long PMMA-loaded SPP waveguide heterointegrated on the rib SOI platform. Error-free performance with power penalty values ranging between 0.2 and 1 dB was obtained for six out of the twelve 40 Gb/s channels, while the rest of them revealed an error-floor at 10^{-7}. The different Bit Error Rate (BER) performance owes to the wavelength-dependent transfer characteristics of the grating couplers and the Erbium-Doped-Fiber-Amplifier (EDFA) response. To the best of our knowledge, this is the first demonstration of the WDM high-throughput data capture and signal integrity credentials of DLSPPs.

2. Experimental setup

Fig. 1 shows the 480 Gb/s WDM-based experimental setup. The outputs of twelve 200 GHz spaced distributed feedback (DFB) lasers operating in the 1542-1560 nm spectral region were multiplexed into a single optical fiber. The multiplexed signal was injected into a Ti:$LiNbO_3$ Mach-Zehnder modulator (MZM) driven by a 40 Gb/s 2^{31}-1

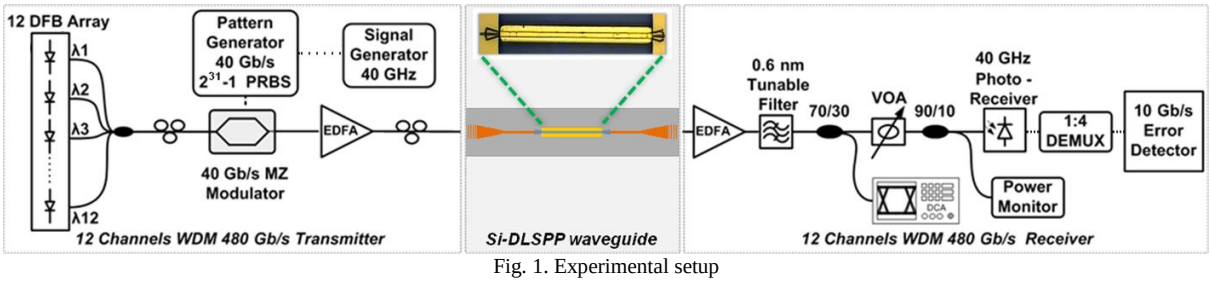

Fig. 1. Experimental setup

Pseudo-Random Bit Sequence (PRBS). The high losses induced by the DLSPP-on-SOI chip were tackled by a combination of one high-power EDFA providing 24 dBm output power and one-low noise EDFA that were placed before and after the chip, respectively. A polarization controller (PC) was also placed at chip's input, ensuring optimum polarization conditions for input light, since the plasmonic waveguides are able to support only Transverse Magnetic (TM) optical mode. After propagation through the straight DLSPPW, the 480 Gb/s WDM signal was amplified by the low-noise EDFA, demultiplexed afterwards into its constituent wavelengths via an optical bandpass tunable filter (OBTF) and subsequently detected by a 40 GHz 3-dB bandwidth photoreceiver followed by an 1:4 electrical demultiplexer. This electrical signal was fed finally into a 10 Gb/s error detector for BER measurements.

The straight DLSPP waveguide used in this experiment was a 60-μm-long PMMA-loaded structure employed in the silicon-plasmonic chip already reported in [2]. The 500-nm-wide and 600-nm-thick PMMA stripe was placed on top of a 3-μm-wide and 65-nm-thick gold film. The SOI motherboard was equipped with TM grating couplers as interfaces for incoming/outgoing signal, each one exhibiting 12 dB insertion loss, and 340×400 nm^2 silicon rib waveguides with 50-nm-thick slab supporting TM light propagation. The SOI-to-DLSPP coupling interface was realized by a butt-coupling approach via tapering the SOI waveguide down to 175 nm width and employing a 200 nm (bottom-to-bottom) vertical offset between the silicon and the gold layer. Moreover, a 500 nm gap was used between the silicon and the DLSPP waveguide in order to ensure its successful realization by taking into account the respective alignment tolerance of the available fabrication equipment. According to chip's cut-back measurements, propagation losses in SOI and DLSPP waveguides and coupling losses per fiber-to-SOI and SOI-to-DLSPP interface were found to be 4.6 dB/cm, 0.1 dB/μm, 12 dB and 2.5 dB, respectively at 1545 nm [2]. Total fiber-to-fiber transmission losses via the chip reached 40 dB at 1545 nm, varying up to 48 dB at 1560 nm as a result of the wavelength-dependent spectral response of the TM grating couplers.

3. Results and discussion

Fig. 2a)-c) depict the spectra of the 12-wavelength data signal before being injected into the Si-plasmonic chip, after exiting the chip and after being amplified by the receiver's EDFA respectively. The WDM signal exiting the chip had different power levels among the twelve channels as a result of the wavelength-dependent transfer function characteristics of the hybrid chip and the EDFA stages. The wavelength dependence of the hybrid chip's spectral response in the spectral band of interest is illustrated in Fig. 2b), showing a non-uniform shape with up to 8 dB differential loss between ch. #1 and ch. #12, which in turn affects the per-wavelength performance of the final amplification stage.

The performance of the 480 Gb/s WDM data transmission over the DLSPPW was evaluated via BER measurements with the corresponding results presented in Fig. 3a)-3f). Back-to-Back (B2B) measurements were received with the replacement of the chip by a variable attenuator that inserted constant, wavelength-independent losses equal to the chip losses experienced by ch. #1-#4 during propagation through the Si-plasmonic path (green line in Fig. 2b)). Fig. 3a) illustrates an overview of BER measurements for all channels. Six channels (ch. #1-#5, ch. #12) achieved error-free operation with their power penalty varying between 0.2 and 1 dB at 10^{-9} error-rate against B2B measurements, whilst the rest of them (ch. #6-#11) exhibited an error-floor at 10^{-7}. Fig. 3b) shows the BER

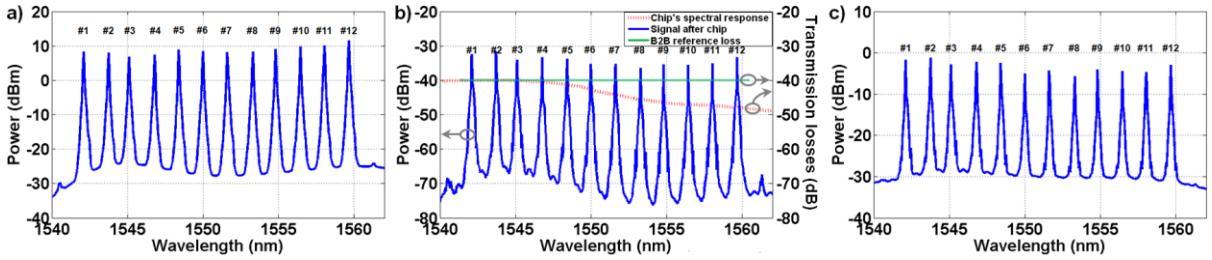

Fig. 2. Spectra of the 12×40 Gb/s WDM signal a) at chip's input, b) at chip's output, in comparison with chip's spectral response and B2B flat losses, c) after post-chip amplification

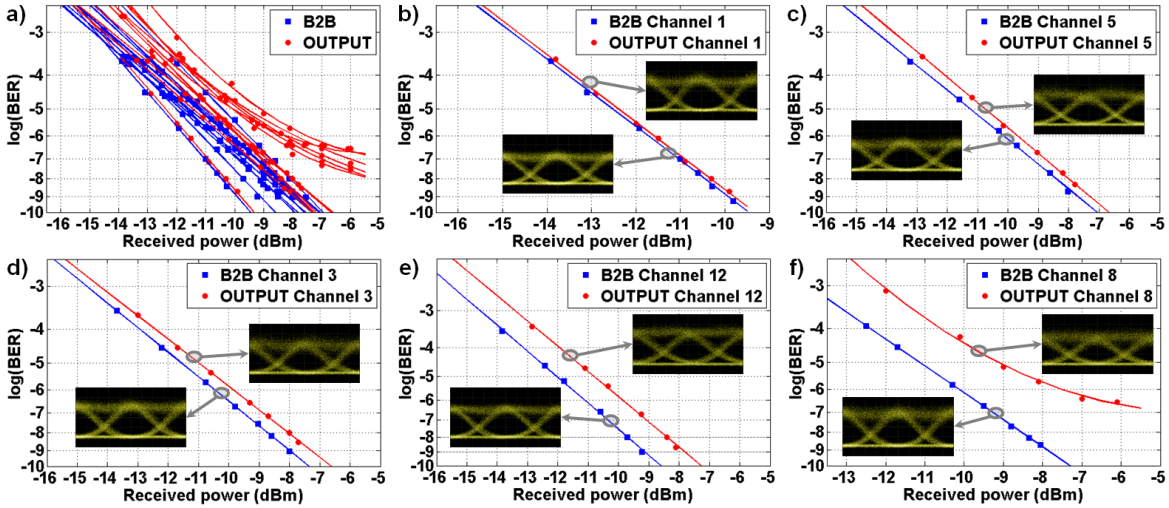

Fig. 3. BER curves for a) all 40 Gb/s B2B and transmitted channels, b) ch. #1, c) ch. #5, d) ch. #3, e) ch. #12, f) ch. #8

curves and the respective eye diagrams for the best performing ch. #1, exhibiting almost equivalent performance against the B2B transmission with only 0.2 dB power penalty that lies within the range of statistical measurement error. Error-free operation with 0.4 dB, 0.7 dB and 1 dB power penalties was also obtained for ch. #5, #3 and #12 respectively, as shown in Fig. 3c)-3e), where also the corresponding eye diagrams are presented. The BER performance and the eye diagrams of the worst performing channel (ch. #8) are depicted in Fig. 3f), showing an error-floor at 10^{-7}. The different power penalties as well as the error-floor performance for the six channels that were not promoted by their spectral location stem from the different optical signal-to-noise-ratio (OSNR) values obtained for each channel as a result of the wavelength-dependent chip and EDFA responses. To this end, the error-floors can be eliminated by selecting all channels to reside within the flat low-loss response of the chip and the employment of gain flattened EDFAs. Finally, single-channel transmission conditions were also investigated, leading to error-free performance with 0.2 dB power penalty for all 12 channels and to BER curves similar to the BER graph shown in Fig. 3b), confirming the high-quality SOI-DLSPP chip performance when wavelength-dependent OSNR values are avoided. In this case, the B2B BER measurements for each individual channel were performed by adjusting every time the B2B reference loss value to the fiber-to-fiber chip losses experienced by the channel being under investigation.

4. Conclusion

We have presented the first WDM-enabled transmission of 0.48 Tb/s aggregate traffic (12×40 Gb/s) through a straight, 60-μm-long DLSPP waveguide integrated on a rib SOI waveguide platform, demonstrating error-free performance for the six channels with power penalty values ranging between 0.2 dB and 1 dB. These results confirm the high-throughput WDM supportive potential of the hybrid SOI-DLSPP waveguide platforms for datacom and computercom interconnect applications [10].

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