

Repetition Rate Multiplication of Pseudorandom Bit Sequences

Christos Kouloumentas, Christos Stamatiadis, *Student Member, IEEE*,
Panagiotis Zakynthinos, *Student Member, IEEE*, and Hercules Avramopoulos

Abstract—We develop a method for the repetition rate multiplication by a factor of 2^n of pseudorandom bit sequences (PRBSs). It makes recursive use of an optical OR-gate in feedback and ensures that the complexity of the resulting circuit is independent of the multiplication factor or the PRBS order to be rate multiplied. We employ an all-optical circuit comprising of two nonlinear fiber Sagnac interferometers and show error-free quadrupling of 12.5-Gb/s PRBSs to 50 Gb/s.

Index Terms—Feedback loop, nonlinear optical loop mirror, nonlinear Sagnac interferometer, optical OR-gate, pseudorandom bit sequence (PRBS), rate multiplication.

I. INTRODUCTION

A recurring difficulty for lightwave technology research groups is the need to upgrade testing infrastructures regularly, as data repetition rates increase. This difficulty is related to the cost and delay in the installation of the new electronics test and measurement equipment and proves insurmountable for less well endowed laboratories.

We take as an example bit-error-rate (BER) test sets. At present the transition from 10- to 40-Gb/s data rates is taking place necessitating the replacement of 10-Gb/s test sets. At the same time, here experiments are being performed at 160 and up to 640 Gb/s [1], [2]. For these rates, all-electronic pattern generation for testing is not available. All-optical pseudorandom bit sequence (PRBS) generation has been shown [3], [4] but an all-optical BER system would require an all-optical error detector that remains to be demonstrated, and in stand-alone form it will not have the programming flexibility of electronic pattern generators. Currently the only practical option is to optically multiplex the pattern provided by electronic pattern generators, in fiber “split-shift-and-recombine” bit interleavers. These interleavers require n stages to obtain 2^n rate-multiplication of the low-rate PRBS [5]. This means that their complexity in terms of components and adjustments scales with the number of stages, while further rate increases require the addition of more stages. It is, therefore, of interest to investigate whether it is possible to rate multiply PRBSs, in a single-stage multiplier, independent of the multiplication factor. In the present communication, we develop such a method.

Manuscript received October 31, 2008; revised December 17, 2008. Current version published March 18, 2009. This work was supported by the European Commission under the ICT EURO-FOS Network of Excellence (Contract 224402).

The authors are with the Photonics Communications Research Laboratory, School of Electrical and Computer Engineering, National Technical University of Athens, 15773 Athens, Greece (e-mail: ckou@mail.ntua.gr; cstamat@mail.ntua.gr; zakynth@mail.ntua.gr; hav@mail.ntua.gr).

Color versions of one or more of the figures in this letter are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/LPT.2009.2013330

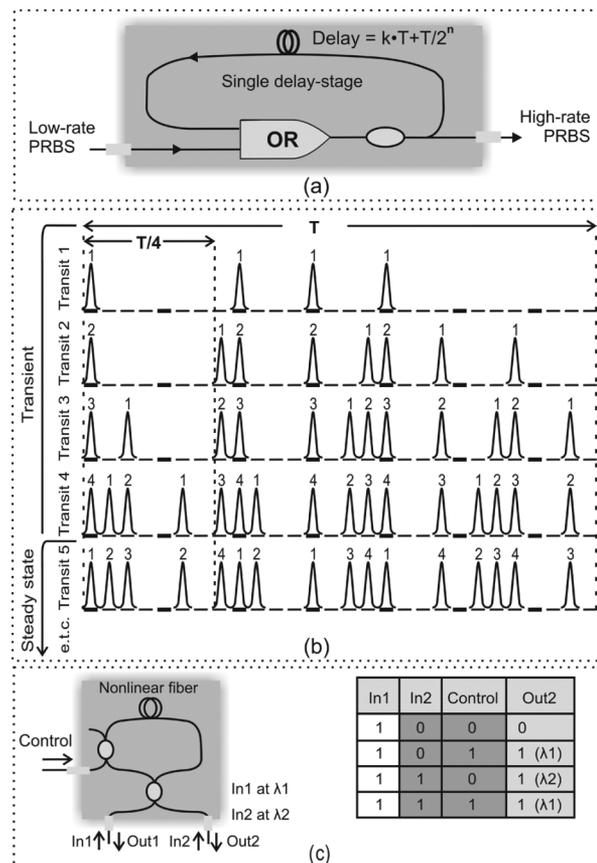


Fig. 1. (a) PRBS rate multiplication concept. (b) Example of rate quadrupling of the $2^3 - 1$ PRBS: the numbers indicate the tributary channel that the pulses belong to. (c) Fiber Sagnac interferometer operating as a 2×2 exchange-bypass switch, and truth table in case of continuous “1s” at In1.

Our method uses an OR-gate in feedback configuration with a delay through the feedback loop such that successive transits build the multiplied PRBS. In this implementation, we use two nonlinear fiber Sagnac loops, one as the OR-gate and the second as the wavelength converter, and quadruplicate a 12.5-Gb/s $2^7 - 1$ PRBS to 50 Gb/s. The resulting PRBS was evaluated by demultiplexing its four interleaved 12.5-Gb/s tributary channels. They were error-free and each exhibited less than 1.5-dB power penalty compared to the input PRBS.

II. OPERATING PRINCIPLE AND EXPERIMENTAL SETUP

Fig. 1(a) shows the scheme in block diagram with the OR-gate and the feedback loop whose purpose is to provide the specified delay between the inputs of the OR-gate. According to the decimation property of PRBSs, in order to achieve a multiplication factor of 2^n of a low-rate input PRBS, the length of the delay must be $T/2^n$, where T is the period of this input PRBS [6]. For

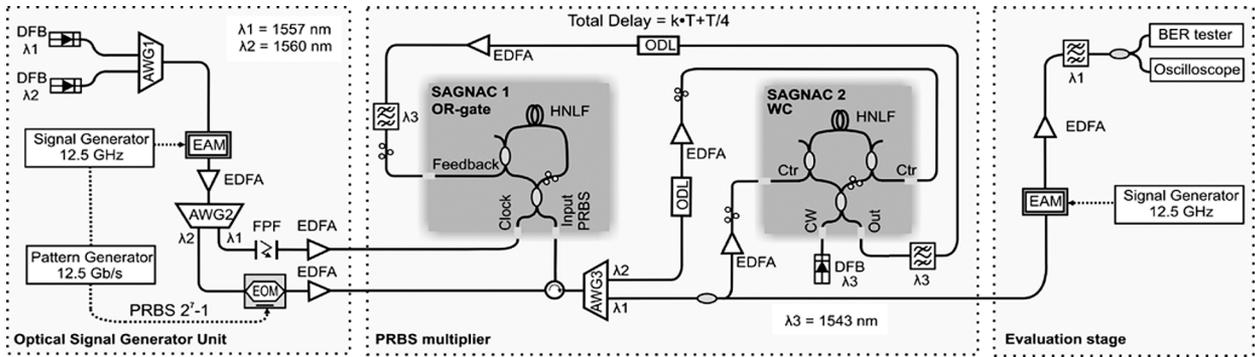


Fig. 2. Experimental setup.

practical reasons, the feedback loop may have to be longer than $T/2^n$, in the general case $k \cdot T + T/2^n$, where k is a nonnegative integer. The scheme effectively “folds” the n stages of the “split-shift-and-recombine” bit interleavers into a single stage and builds the rate-multiplied PRBS after 2^n transits through the gate, thereafter reproducing it indefinitely.

Fig. 1(b) shows, as an example, the rate quadrupling of a $2^3 - 1$ PRBS (1011100) with this concept. After the first OR operation, the loop contains the input PRBS. In the next $2^n - 1(3)$ transits through the gate, the pulses arriving through the feedback path are delayed with respect to the input PRBS by one quarter of its period and are ORED with it, each time occupying adjacent slots of the final bit stream. After a total of $2^n(4)$ OR operations or $2^n - 1(3)$ transits through the feedback loop, the rate-multiplied PRBS is created, containing $2^n(4)$ interleaved, low rate PRBSs. The temporal window that was originally occupied by a single period of the low-rate PRBS is now occupied by 2^n periods of a PRBS of the same order but with 2^n higher repetition rate. In Fig. 1(b), the four channels are indicated by the numbers on top of the pulses. From that point onwards, the OR-gate reproduces the same pattern and the circuit reaches a steady-state. In principle this method can be applied to any multiplication factor 2^n or PRBS order.

In our implementation, the OR operation was obtained with a 2×2 exchange-bypass switch [7], realized with a nonlinear Sagnac loop as in Fig. 1(c). Depending on the control signal, the switch operates in the bar or cross state. In the absence of a control pulse, both inputs are mirrored out to their incoming ports, whereas if a control pulse is present they are switched over. As shown in the truth table of Fig. 1(c), if a stream of “1s” enters In1, the result of the OR-operation between the other input, In2, and the control signal appears at the Out2 port. Input signals into ports In1 and In2 were the optical clock at the final rate and wavelength λ_1 , and the low-rate PRBS at wavelength λ_2 , respectively. The control signal was the feedback stream. Since the control signal must be at a different wavelength λ_3 from the inputs at λ_1 or λ_2 , the output signal in Out2 must be wavelength converted before returning as feedback signal.

Fig. 2 shows the experimental setup. It consists of the signal generation unit, the PRBS rate multiplier unit and the evaluation stage. The outputs of two distributed-feedback (DFB) laser diodes at λ_1 (1557 nm) and λ_2 (1560 nm) were modulated in an electroabsorption modulator (EAM) to provide pulsetrains of 7 ps at 12.5 GHz. The pulsetrain at λ_1 entered a fiber Fabry-Pérot filter (FPF) with 50-GHz free-spectral range (FSR) and finesse of 100. This output pulsetrain provided the 50-GHz optical clock signal and exhibited amplitude

modulation of about 1 dB. The second pulsetrain at λ_2 was modulated in a Li:NbO₃ electrooptical modulator (EOM) by a $2^7 - 1$ PRBS. The 50-GHz clock and the 12.5-Gb/s PRBS were amplified in erbium-doped fiber amplifiers (EDFAs) and entered SAGNAC1 as input signals. The nonlinear element was 180 m of highly nonlinear fiber (HNLF) with 1.21-ps/nm/km dispersion and $10\text{-W}^{-1}\text{km}^{-1}$ γ parameter. At the output port of SAGNAC1, the signals at wavelengths λ_1 and λ_2 were wavelength converted to λ_3 (1543 nm) in SAGNAC2. They were separated with arrayed waveguide grating (AWG3), and entered SAGNAC2 as control signals in a counterpropagating configuration, with their relative timing preserved. The nonlinear element of SAGNAC2 was 260 m of the same type of HNLF as in SAGNAC1. The average power of the control signals at λ_1 and λ_2 was limited by the available EDFAs to 240 and 70 mW, respectively, and resulted in about 70% switching of SAGNAC2. The wavelength-converted signal at λ_3 closed the feedback loop as control signal of SAGNAC1. It was arranged to arrive delayed by $k \cdot T + T/4$ with 620-mW average power. The 50-Gb/s PRBS output was obtained from AWG3 as the λ_1 output of the OR gate, and it was evaluated by demultiplexing its four tributary channels.

III. RESULTS AND DISCUSSION

Fig. 3(a)-(b) illustrates traces and eye-diagrams of the 12.5-Gb/s input $2^7 - 1$ PRBS obtained after the EOM and the 50-Gb/s output PRBS after AWG3, and reveals that the correct pattern was obtained. Fig. 4(a) shows traces of the four 12.5-Gb/s interleaved PRBSs after demultiplexing with an EAM, and the complete 50-Gb/s PRBS depicted with the same trigger signal. The four channels have the same pattern form as the input PRBS. They were obtained by successively delaying the signal in the EAM by 20 ps each time. Union of the four 12.5-Gb/s traces yields the 50-Gb/s sequence on the bottom of Fig. 4(a). In Fig. 4(b), we present the BER curves obtained for the low-rate PRBS as back-to-back (B-2-B) measurement and the four 12.5-Gb/s channels after demultiplexing. Error-free operation was achieved for all channels with power penalty of less than 1.5 dB relative to the input PRBS, and less than 0.3-dB variation between them. The primary reason for this penalty was the 1-dB modulation in the FPF generated clock signal and the insufficient power provided by the amplifier in the control signal of SAGNAC2. In combination, these two constraints did not allow for effective signal regeneration in the circuit. As a result the optical signal-to-noise ratio degradation by 5 dB of the 50-Gb/s PRBS signal compared to the input 12.5-Gb/s signal could not be corrected. By modifying the feedback

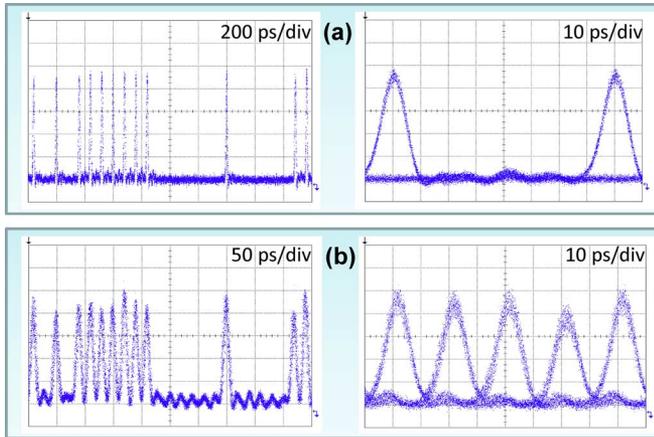


Fig. 3. (a) and (b) Traces and eye-diagrams of input 12.5 Gb/s and rate multiplied 50-Gb/s PRBS.

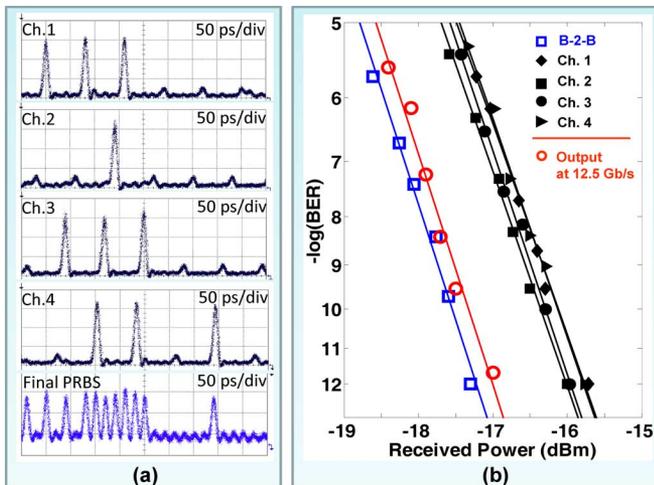


Fig. 4. (a) Traces of the four tributary channels after demultiplexing. Bottom trace is the 50-Gb/s PRBS. (b) BER curves of four tributary channels and input, B-2-B, 12.5-Gb/s PRBS. BER data of output 12.5-Gb/s PRBS obtained from quadrupled 3.125-Gb/s PRBS is also shown with empty circle curve.

delay, the circuit was also used for the rate multiplication of the $2^3 - 1$ PRBS from 12.5 Gb/s to 50 and 25 Gb/s, and similar results were obtained. To verify that the PRBS generated at the aggregate rate is also error-free, we have quadrupled a 3.125 Gb/s $2^7 - 1$ PRBS. The optical signal generator unit of Fig. 2 was modified to provide directly the 12.5-GHz optical clock signal and the 3.125-Gb/s PRBS pattern. This ensured a good quality optical clock signal and enough power to fully switch the SAGNAC gates. The BER curve with the open circles of Fig. 4(b) shows a power penalty of only 0.2 dB of the rate multiplied output PRBS, compared to the 12.5-Gb/s optical PRBS obtained directly from the electronic PRBS generator (B-2-B).

The circuit was stable for characterization when care was taken to prevent temperature fluctuations in the laboratory and to protect the polarization sensitive parts from random air drifts. Error-free operation could be sustained provided that variations in the delay of its feedback path were within ~ 1 ps of the optimum value.

TABLE I
INDICATIVE REQUIRED LENGTHS OF THE FEEDBACK LOOP (IN METERS)

PRBS order	40 Gb/s	160 Gb/s	320 Gb/s	640 Gb/s	640 Gb/s
7	($k=322$) 818.52	($k=290$) 696.12	($k=274$) 675.72	($k=262$) 665.52	($k=1032$) 2621.32
9	($k=80$) 820.16	($k=72$) 695.60	($k=68$) 674.83	($k=65$) 664.46	($k=256$) 2616.48
11	($k=20$) 829.04	($k=18$) 698.54	($k=17$) 656.31	($k=16$) 655.68	($k=64$) 2620.80
15	($k=1$) 819.18	($k=1$) 696.30	($k=1$) 675.82	($k=1$) 665.58	($k=4$) 2631.60
23					($k=0$) 2621.44

To explore the versatility of our method, we investigated the feedback delay required to obtain other PRBS orders and multiplication factors. Table I summarizes indicative delay lengths for multiplication of several 10-Gb/s PRBS orders to a variety of final bit rates. It was obtained on the assumption that a 5-ns propagation delay corresponds to 1-m fiber length. Table I shows that multiplication of orders up to 15 can be easily accommodated up to 640 Gb/s. Moreover, the parameter k in $k \cdot T + T/2^n$ can be chosen so that the lengths for the PRBS orders in the same multiplication factor family lie in close proximity. The down-scaling of the required delay as the multiplication factor increases, enables the multiplication of the $2^{23} - 1$ PRBS to 640 Gb/s with a realistic length of about 2621.44 m. Again, k can be appropriately modified to allow for the required delays of all PRBS orders to lie in close proximity. Finally, for higher repetition rate multiplication factors, the power requirements for the SAGNAC gates are expected to remain the same, provided that the duty-cycle of the optical pulses at the final rate is also retained.

IV. CONCLUSION

We have demonstrated a method to rate-multiply a PRBS by a factor of 2^n that makes recursive use of an optical OR-gate in feedback. A circuit comprising of two nonlinear fiber Sagnac interferometers was used to obtain error-free quadrupling of 12.5-Gb/s PRBSs to 50 Gb/s.

REFERENCES

- [1] M. Galili, L. K. Oxenlowe, H. C. H. Mulvad, A. T. Clausen, and P. Jeppesen, "Optical wavelength conversion by cross-phase modulation of data signals up to 640 Gb/s," *IEEE J. Sel. Topics Quantum Electron.*, vol. 14, no. 3, pp. 573–579, May/June 2008.
- [2] H. C. H. Mulvad, E. Tangdionga, O. Raz, J. Herrera, H. De Waardt, and H. J. S. Dorren, "640 Gbit/s OTDM lab-transmission and 320 Gbit/s field-transmission with SOA-based clock recovery," in *Proc. OFC 2008*, San Diego, CA, Feb. 2008, Paper OWS2.
- [3] A. J. Poustie, K. J. Blow, R. J. Manning, and A. E. Kelly, "All-optical pseudorandom number generator," *Opt. Commun.*, vol. 159, pp. 208–214, Jan. 1999.
- [4] L. Christen, O. Yilmaz, S. Nuccio, X. Wu, and A. E. Willner, "Optical pseudo-random bit sequence generator using a dual-drive Mach-Zehnder modulator as a linear feedback shift register," in *Proc. LEOS 2008*, Newport Beach, CA, Nov. 2008, Paper TuP3.
- [5] S. A. Hamilton, B. S. Robinson, T. E. Murphy, S. J. Savage, and E. P. Ippen, "100 Gb/s optical time-division multiplexed networks," *J. Lightw. Technol.*, vol. 20, no. 12, pp. 2086–2100, Dec. 2002.
- [6] P. H. Bardell, W. H. McAnney, and J. Savir, "Pseudorandom sequence generators," in *Built-In Test for VLSI: Pseudorandom Techniques*. New York: Wiley, 1987, ch. 3, pp. 61–88.
- [7] G. Theophilopoulos *et al.*, "Optically addressable 2×2 exchange bypass packet switch," *IEEE Photon. Technol. Lett.*, vol. 14, no. 7, pp. 998–1000, Jul. 2002.