Bit- and Packet-Level Self-Synchronization for All-Optical Label-Switched Network Nodes with Transparency to Network-Traffic

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Abstract: We demonstrate a self-synchronization sub-system that produces bit and packet-level signals to all-optical label-switched nodes. The circuit uses a comb-generating filter and two integrated optical gates and operates with asynchronous and variable-length packets.

OCIS codes: (060.2330) Fiber optics communications; (230.1150) All-optical devices; (250.5980) Semiconductor Optical Amplifiers; (050.2230) Fabry-Perot

1. Introduction and Concept

The migration from circuit-switched WDM networks to optical packet-switched networks (OPS) has been identified as a key issue for realizing future optical networks delivering bandwidth-on-demand and triple-play applications. New switching paradigms, such as Multiprotocol Label Swapping (MPLS) [1] and all-optical label swapping (AOLS) have been recently introduced for solving the mismatch between fiber capacity and router packet forwarding capacity [2]. The application of optical signal processing techniques to realize intelligent network functionalities has become feasible due to the development and commercialization of high-speed optical switching elements, such as Semiconductor Optical Amplifier Mach-Zehnder Interferometric (SOA-MZI) optical gates [3]. The current research thrust, within European IST-LASAGNE project, is towards the realization of a truly photonic router, performing all switching and forwarding functionalities in the optical layer [4]. A crucial parameter dictating the potential for deployment of such an all-optical router is its cost-effectiveness. The use of a single fundamental building block such as the SOA-MZI for building the complete node avoids the requirement for custom-made technological solutions within the node and allows for a common fabrication procedure for all node sub-systems, reducing the overall cost. Moreover, integration of arrays of such optical gates onto the same chip, currently researched within European IST-MUFINS project [6], further reduces the cost of the required photonic devices, which are dominated by packaging and pigtailing.

Figure 1(a) shows a block diagram of the basic functionalities required to realize an AOLS router, namely synchronization, regeneration, label processing and data forwarding. In LASAGNE all functionalities are handled in the optical domain exploiting the processing power and high-speed operation of optical gates. In the case of synchronization, in order to simplify transmission and optimize performance in the AOLS network, each node should be able to locally generate all the signals required for bit- and packet-rate synchronization. The clock recovery sub-system performs bit-level synchronization [5] and is used for 3R regeneration of the incoming traffic, whereas the packet synchronizer extracts a single pulse per incoming packet and is used for providing all the local signals for powering and driving subsequent gates and sub-systems, such as the label recognition and the local address generation sub-systems. Previous reported results on single pulse extraction employed a marker pulse in different wavelength [7] or polarization [8]. These techniques result in increased complexity in the packet transmitter and high sensitivity due to fiber transmission. More recently, a single SOA with long recovery time has been used, which, requires strict line coding schemes [9] and specific packet formats [10] for correct operation.

In the present communication we demonstrate a method for all-optical synchronization generating a packet clock and a single pulse on a per-packet basis. The subs-system is realized using hybrid integrated Mach-Zehnder Interferometers (HMZI) and does not require a marker pulse or data coding schemes, such as Manchester encoding. The reported packet-synchronizer operates with conventional Return-to-Zero modulation, irrespective of the packet length for both synchronous and asynchronous packet-mode traffic.

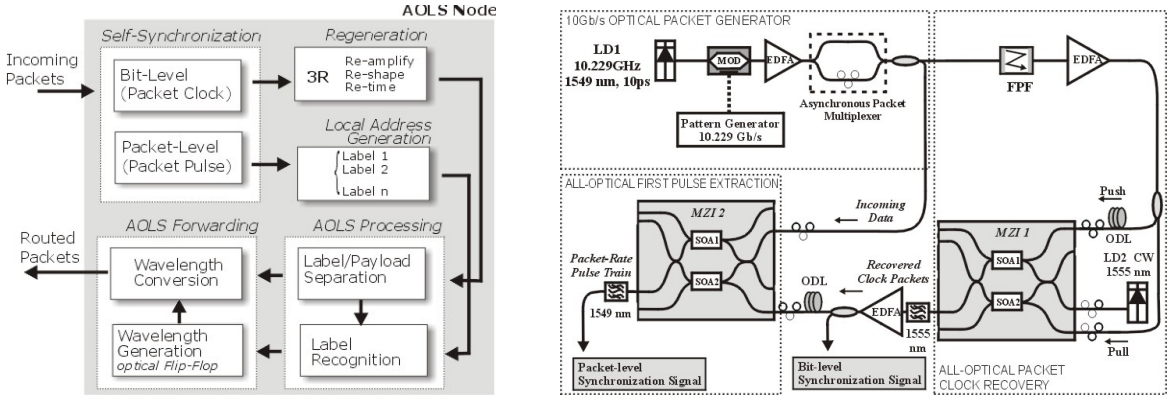

Fig. 1. (a) General block diagram of an AOLS node and (b) experimental setup of packet self-synchronization subsystem.

2. Experimental Setup

The experimental setup consists of the 10 Gb/s optical packet generator, the packet clock recovery and the packet synchronizer, as depicted in Fig. 2. The input signal was generated by a DFB laser diode (LD 1) at 1549 nm, gain-switched at 10.229 GHz to provide 10 ps pulses after linear compression. This pulse-train was modulated into data packets of variable-length containing a 2^7-1 PRBS data pattern, produced by a programmable pattern generator, driving a Ti:LiNbO3 modulator. For the synchronous operation the pattern generator was programmed to generate two consecutive packets of 40 bits and 134 bits, repeating every 24.83 ns, a period equivalent to a packet rate of 40.27 MHz. Asynchronous packet flow was achieved by increasing the period of the same packets to 49.66 ns and by interleaving the packets through the asynchronous packet multiplexer, as shown in the dashed box of Fig. 2. Fine adjustment of the phase alignment was achieved by employing a variable optical delay line (ODL) in one path of the multiplexer. The generated data packet signal was divided in two parts, one inserted in the packet clock recovery module and the other used in the packet synchronizer. The clock recovery circuit employed a Fiber Fabry-Pérot Filter (FFP) with Free Spectral Range (FSR) equal to the line rate and Finesse of 47 and a optical gate (MZI1) powered by a CW signal at 1555 nm (LD 2), operating as a holding beam. The FFP filter acts as a passive optical resonator that extracts the line rate spectral components of the input signal. The exponentially decaying impulse response of the filter converts the incoming data packets into clock packets with intense pulse amplitude modulation and duration that is similar to that of the incoming packets. HMZI 1 is saturated by the injection of the CW light and yields a power-limiting transfer function [12] reducing the intensity modulation and providing a good quality packet clock signal. A push-pull configuration was adopted in order to reduce the switching window of the HMZI. The clock packets then served as the control signal in the following HMZI (MZI 2), to extract the leading pulse of each incoming data packet at the switched output port of the switch. Finally the output packet-rate pulse train was filtered by a 1nm band pass filter to remove out-of-band noise from the SOAs.

3. Results and Discussion

Typical results for synchronous and asynchronous variable-length packets are shown in Fig. 2 and 3. Figure 2(a) depicts the leading part of the 134-bit input data packet and fig. 2(d) a sequence of two asynchronous packets, each having different length. Fig 2(b) shows the corresponding recovered clock packets at the output of MZI 1 and fig. 2(e) shows the two asynchronous recovered clock packets. The clock recovery displays a sharp lock-in time of 2 bits, whereas it falls to 1/e within 15 bits. Best operation of the clock recovery HMZI gate was achieved with 790 μW of optical power from the CW source, 200 fJ/pulse for the push and 178 fJ/pulse energy for the pull control signal. Fig. 3(c) and (f) show successful extraction of the packet pulse. The extinction ratio at MZI 2 between the extracted pulses and the following packet bits was in excess of 10 dB and the circuit required 22 fJ/pulse for the incoming data packets and 80 fJ/pulse for the clock packet control signal. Figure 3 shows the measured eye diagrams of the packet synchronizer. Figure 3(a) and (c) show the incoming data packets at 10 Gb/s for synchronous and asynchronous operation respectively. Figure 3 (b) and (d) show clear and open eyes of the extracted packet pulse for both types of traffic. The packet-synchronizer introduces short guardbands irrespective of

the incoming packet length defined by the clock recovery circuit. The packet clock rise and decay times determine the minimum intra-packet time interval and are equal to the total guardbands. The total bandwidth overhead decreases as the packet length increases and is 10% for 13 ns packets and reduces to 8% for ATM packets.

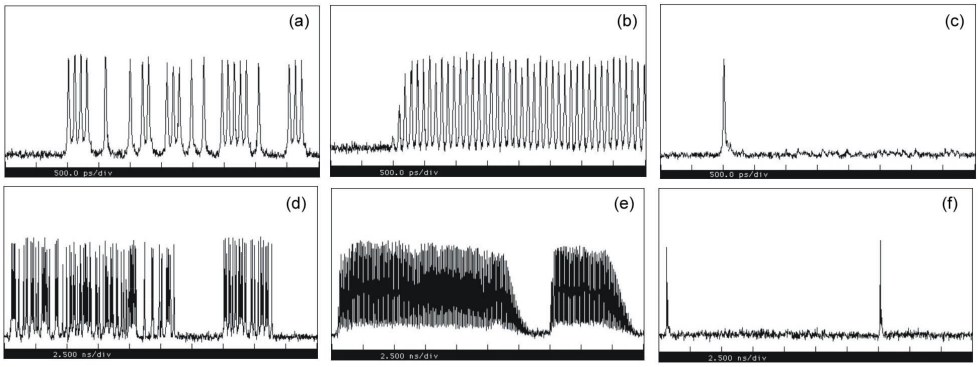

Fig. 2. (a), (b), (c) Synchronous input data packets, clock packets and extracted pulse (time base 500 ps/div) and (d), (e), (f) asynchronous and variable-length data packets, clock packets and extracted packet pulse (time base 2.5 ns/div)

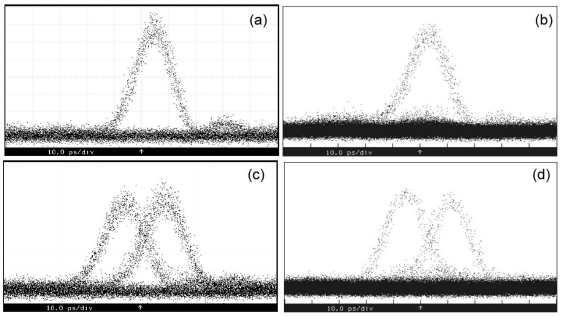

Fig. 3. Eye diagrams (10ps/div) of (a), (c) input data and (b), (d) extracted single pulse for synchronous and asynchronous operation.

4. Conclusion

We have presented an all-optical sub-system capable of generating packet and bit- level synchronization signals for short asynchronous and variable-length packets for use in the front-end part of an all-optical label-switched router. The technique employs a Fiber Fabry-Pérot Filter and an integrated MZI to implement the packet clock signal generation and an additional hybridly integrated MZI to generate a single pulse per incoming packet. The scheme is based on optical filtering and integrated switching elements, requires no high-speed electronics and provides high bandwidth efficiency. Given that the clock recovery circuit and the HMZIs have been shown to operate at 40 Gb/s [3,5], the circuit is upgradeable to higher rates.

References

[1] E. Rosen et al., IETF Request of Comments, RFC 3031, Jan. 2001
[2] D. J. Blumenthal, "Optical Packet Switching", in ECOC 2004, Th1.6.1
[3] A. Poustie, "Semiconductor Devices for All-Optical Signal Processing", in Proc. ECOC 2005, pp. 475-478
[4] F. Ramos et al., "IST-LASAGNE: Towards All-Optical Label Swapping Employing Optical Logic Gates and Optical Flip-flops", IEEE/OSA J. Lightwave Technol., to be published, Nov. 2004
[5] L. Stampoulidis et al., "40 Gb/s Fast-Locking All-Optical Packet Clock Recovery", in OFC 2005, O.Th.E.2.
[6] http://mufins.cti.gr
[7] Y. Shimazu and M. Tsukada, "Ultrafast photonic ATM switch with optical output buffers," J. Lightwave Technol., 10, 265–272 (1992).
[8] I. Glesk, et al., "All-optical address recognition and self-routing in a 250 Gbit/s packet-switched network," Elec. Lett., 30, 1322–1333 (1994)
[9] H. J. Lee et al., "A simple packet level clock extraction scheme using a terahertz optical asymmetric demultiplexer," IEEE Photon. Technol. Lett., 11, 1310–1312, (1999)
[10] N. Calabretta et al., "Optical Signal Processing Based on Self-Induced Polarization Rotation in a Semiconductor Optical Amplifier", IEEE J. Lightwave Technol., 22, 372-381, (2004)

Acknowledgments

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