Software tools for photonic integrated circuit design using "monolithic-on-hybrid" integration

Twan Korthorst [a], Paraskevas Bakopoulos [c], Remco Stoffer [a], Efstratios Kehayas [c], Graeme Maxwell [b], Hercules Avramopoulos [c]

[a] *PhoeniX Software, P.O. Box 545, 7500AM Enschede, The Netherlands*
e-mail: twan.korthorst@phoenixbv.com
[b] *CIP, B55, Adastral Park, Martlesham Heath, Ipswich, IP5 3RE, United Kingdom*
[c] *National Technical University of Athens, 9 Heroon Polytechniou Str, 157 73 Zografou, Athens, Greece*

The increasing demand for high capacity in optical networking is posing ambitious targets in all segments of the network. In the metro/access networks the focus of attention is on re-configurability, whereas in the core networks research is targeting both transmission bit rate and advanced modulation formats. It is widely accepted that a viable route to achieve such performance requirements with reasonable cost is through photonic integration. In this rationale, the target is to increase the scale of integration both horizontally (increase on-chip functionality) and vertically (increase on-chip channels) so as to develop complex large-scale Photonic Integrated Circuits. So far, large-scale PICs have been fabricated through monolithic [1] or hybrid [2, 3] integration techniques. European project APACHE aims at creating the methodology in order to blend these technologies and combine their merits. In this "monolithic-on-hybrid" approach, arrays of monolithic components (lasers, modulators, amplifiers) are passively assembled on a silicon submount (daughterboard) which is in turn passively assembled into the planar silica motherboard (figure 1). By fine tuning the balance between monolithic and hybrid integration (select the size and number of the monolithic arrays on the hybrid chip) device yield can be optimized, whereas different types of PICs can be fabricated without the need for a complete re-design. This paper describes the software tools that are under development in order to facilitate the design and fabrication of "monolithic-on-hybrid" large-scale PICs.

Succesfull research and development of micro and nano engineered products relies on an integrated design and fabrication flow incorporating design, process development, fabrication and measurements (see figure 2). Contrary to the IC-industry the fabrication process (process flow) of the actual devices is a key parameter of the design. In a simplified way a designer in the IC industry has a two-dimensional design space (creating functionality by routing metal patterns), whilst a full three-dimensional design approach is required in the current status of the micro and nano engineering industry (creating functionality by etching fluidic channels, depositing optical waveguides, etc.). The creative process of the designer should be supported by a design methodology and corresponding tools providing the fabrication technology parameters (geometrical information and performance) integrated with the required physical simulations.

Currently, there are no commercially available integrated design tools for micro and nano engineering. There are lots of commercial pieces of software and home built programs available, however none of them is capable of supporting the design work in an integrated manner. Furthermore there are no simulation tools for complex photonic integrated circuits involving non linear active and passive devices. There are several reasons why this situation exists – the intrinsic requirement in photonic integration to marry together devices from dissimilar material systems and hence differing design rules; a more fragmented industry where individual companies carry out their own fabrication rather than outsourcing; and an industry that is still dominated by discrete components rather than integrated circuits.

In the framework of the work presented (see figure 2), sophisticated parametric chip design tools and novel 3D simulation tools [4] have been designed and developed, enabling efficient modelling of the different material systems. Future work will incorporate a non linear active material model based on simple S-matrix and/or Rate equations and validated with the actual performance of fabricated structures and devices. Furthermore the existing design tools will be extended with additional functionality to combine designs from the different material domains, supported by auto-routing and standard parametrised libraries. This will include the actual manufacturing process tolerances and the influence of these on the actual performance.

Acknowledgements
The work described in this paper was carried out with the support of the APACHE-project ("Agile Photonic Integrated Systems-on-Chip enabling WDM Terabit Networks"), a Specific Targeted Research Project funded by the European Commission through the 7th ICT-Framework Programme.

References

[1] R. Nagarajan et al, "Single-chip 40-channel InP transmitter photonic integrated circuit capable of aggregate data rate of 1.6 Tbit/s", IEE Electron. Let, Vol. 42, No. 13, Jun. 2006.
[2] G. Maxwell, "Hybrid Integration Technology for High Functionality Devices in Optical Communications", invited paper OWI3, OFC 2008, San Diego, U.S.A. (2008).
[3] http://www.ciphotonics.com
[4] R. Stoffer and J. Bos, "Fixed-grid Finite Element Beam Propagation Method", oral presentation at the XVIIth International Workshop on Optical Waveguide Theory and Numerical Modelling, Eindhoven, the Netherlands (2008).

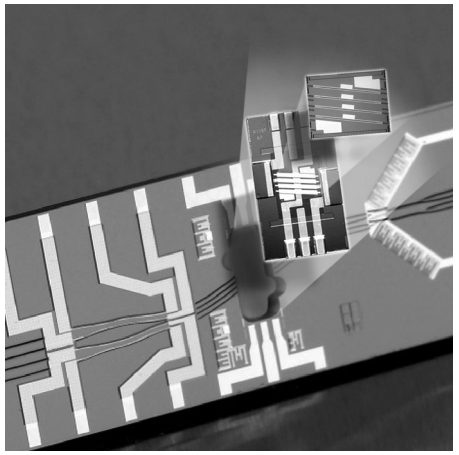

Figure 1.Hybrid integration concept of active (InP) and passive (silicon) components onto a silicon motherboard.

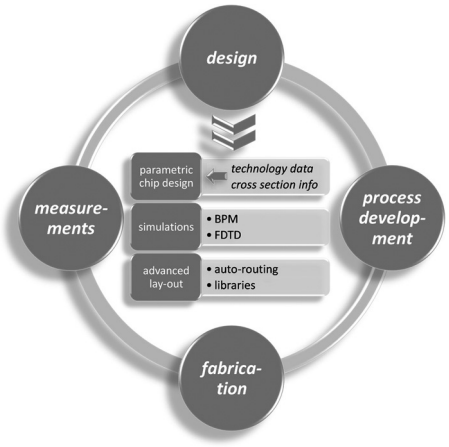

Figure 2. Schematic overview of the integrated design and fabrication flow.