20 Gbps BOOLEAN XOR WITH UNI GATE

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***Abstract**: We demonstrate Boolean XOR at 20 Gbit/s using a Semiconductor Optical Amplifier-based Ultrafast Nonlinear Interferometer (UNI). The gate demonstrates low pattern dependence and very low switching energies.*

Introduction

The rapid increase in bandwidth demand on telecommunications carriers has resulted in continuing effort to increase the single channel transmission line rate /1/. In order to make practical use of these achievements, it is necessary to be able to carry simple logic operations in the optical domain at the line rate and this in turn has intensified interest in all-optical, ultra-high speed, digital logic and switching /2-3/. Switching devices based on semiconductor optical amplifiers (SOA's) have attracted a lot of attention due to their low switching energies and latencies /4-7/. Recently, a single-arm Ultrafast Nonlinear Interferometer (UNI) gate using a SOA has been demonstrated /8/, being capable of Boolean AND up to 100 Gbit/s /9/.

For the realization of ultra-high speed, all-optical, signal processing systems, capability to perform dual rail logic operations and in particular Boolean XOR is crucial to build systems such as binary adders /10/, data encoders, encryption and comparator circuits. So far the XOR capability has been demonstrated with a SOA-assisted Sagnac gate at up to 10 Gbps /11/. In this communication we report the demonstration of XOR operation at 20 Gbps using the UNI gate with pseudo-data control patterns. Low switching energies and low pattern dependence in the switching is shown.

Experiment

In the present experiment three optical signals were used as inputs into the gate. Controls A and B are the logical inputs to the switch controlling its state while CLK is the clock input. The outcome of the logic XOR of A, B is imprinted on CLK, which is held continuously to a logical 1 on input to the gate. Fig.1 shows the experimental setup. The three optical signals were produced by two packaged, fibre pigtailed, gain switched DFB semiconductor diode lasers, LD1 and LD2, operating at 1545.2 nm and 1554.6 nm. They were driven from a synthesised RF signal generator at 10 GHz and produced 9 ps pulses after linear compression with a dispersion compensating fiber of total dispersion –47 ps/nm. LD1 provided the optical clock signal and control A and LD2 provided control signal B. The performance of the gate was evaluated for several control data patterns.

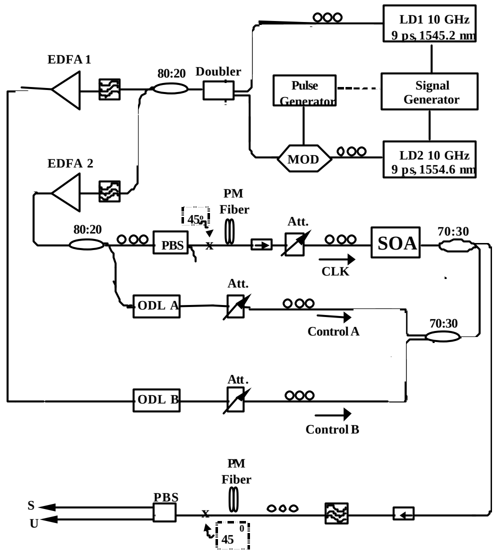

Figure 1: Experimental Setup

Here we show results for control A as a 20 GHz full duty cycle control and control B a 20Gbps pseudo-data signal obtained using a $LiNbO_3$ modulator, driven from a programmable pulse generator. The repetition rate of the three optical signals was doubled by bit interleaving in a split-relative-delay-and-recombine fiber doubler. The 32 bit-long pseudo-data pattern used in control B, consisted of the sequence 01010101011111111010101010000000. The signals from LD1 and LD2 were separated after the repetition frequency doubler with 2 nm tunable filters to form the three optical signals interacting in the UNI and were next amplified in EDFA2 and EDFA1 respectively. Optical power control of the three signals was provided with variable attenuators at the input of the gate. The UNI gate consists of a fiber polarization beam splitter (PBS) followed by 12 m of polarization maintaining fiber spliced at 45^0 at the output pigtail of the PBS. This allows for a 25 ps relative delay between the two orthogonal polarizations resulting from the CLK signal as they enter the SOA. In the present implementation controls A and B were brought in counter-propagating direction from the CLK pulse train and were precisely synchronised in the SOA with the delayed components of the clock, using two variable delay lines, ODL A and ODL B. The purpose of these control pulses is to impose a local, time dependent, refractive index change in the SOA so as to to ensure a relative phase change between the two orthogonal components of the CLK signal. On exiting the SOA, the CLK signal is filtered in a 5 nm filter. The relative delay between the orthogonal components of the CLK pulses is removed by employing an identical length of PM fiber to that used at its input and finally the two components are made to interfere in a fiber PBS with its axes spliced at 45^0 to the PM fiber. The active switching device was a 1.5 mm long bulk InGaAsP-InP ridge waveguide SOA, with peak small signal gain of 30 dB at 1558.9 nm when driven with 750 mA current and 80 ps recovery time. Isolators were used at the ports of the SOA to eliminate undesirable reflections and polarization controllers were used in the input CLK and control ports of the UNI for polarization state optimization.

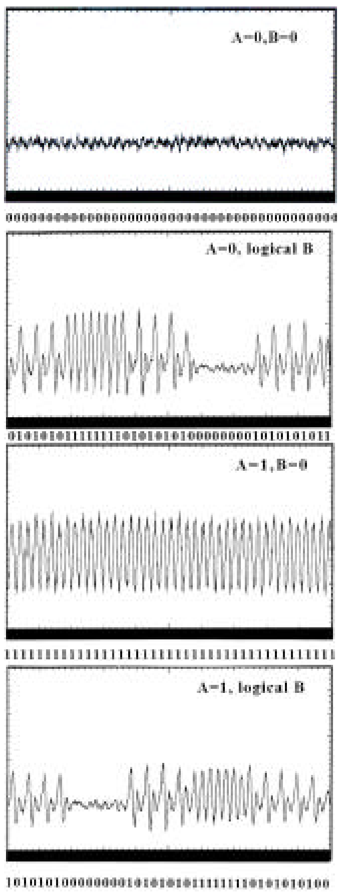

Figure 2: Switched port outputs for the four logical combinations of A and B.The time-base is 200 ps.

Results and discussion

In the absence of any control pulses the CLK signal appears unswitched in the U port of the PBS. If either of the control pulses is present, the UNI operates as an AND gate and the signal appears in the switched port S. This means that for successful Boolean XOR operation between A and B, the switched port of the gate must record a logical ‘1’ if either A or B is ‘1’ and a logical ‘0’ if both A and B are ‘1’ or ‘0’. Fig. 2 illustrates the logic output of the gate with data for the four logical combinations of control A and B. Bit by bit checking proves that correct XOR operation has been obtained. The gate has been evaluated with different control patterns and has always performed XOR successfully. The contrast ratio between the ON-OFF states of the gate was as high as 6:1 and the energies of clock, control A and control B pulses were 2.5 fJ, 15 fJ and 4 fJ respectively. Note that the trailing control pulses B have less energy than the preceding pulses A in order to balance out the heavier gain saturation of the SOA, so that the orthogonal components of CLK signal experience the same gain. These switching pulse energies are indeed low and make conceivable the use of the UNI in a loss-optimised logic circuit, even without the use of pre-amplification of the optical signals before interaction in the gate. The temporal window within which the contrast of the switched signals degrades by 3 dB as the optical signals are mis-timed was found to be 30 ps, indicating tolerance of the device to incoming signal timing jitter /12/.

Conclusions

In conclusion we have demonstarted for the first time to our knowledge Boolean XOR with a semiconductor-based, intereferometric, UNI gate at 20 Gbps. Bit pattern switching was achieved with very low pulse energies, low pattern dependence and over a broad switching window. It is expected that the use of shorter pulse train signals will extend the XOR capability of the UNI to higher rates.

Acknowledgements

The authors gratefully acknowledge partial support for this work by the CEC via the ESPRIT programme, project 36078 DO_ALL, and by the Swiss Federal Office for Education and Science.

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