20 Gb/s All-Optical XOR with UNI Gate

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Abstract—All-optical Boolean XOR is demonstrated on a 20 Gb/s pseudodata pattern using a semiconductor optical amplifier-based ultrafast nonlinear interferometer (UNI) switch. Bit pattern switching with low-pattern dependence and low switching energies is achieved.

Index Terms—All-optical Boolean XOR, high-speed logic, optical gates, ultrafast nonlinear interferometer (UNI).

I. INTRODUCTION

THE effort toward extending the single-channel transmission rate envelope is continuing unabated [1]. One reason for this is the significant cost reduction that may be achieved due to the reduction of the line card count at the terminal equipment and the simplification of transmission hardware control and management. In order for such transmission rates to become practically realisable, it is imperative that some low-level ultrahigh-speed signal processing is done at the line rate. Over the years a number of ultrahigh-speed, all-optical, nonlinear switching and logic arrangements have been demonstrated. Early work has concentrated on the exploitation of the optical Kerr effect in fiber interferometers [2]–[5]. More recent devices use the nonlinear carrier dynamics in semiconductor optical amplifiers (SOA's), due to their low switching energies and short latencies [6]–[9]. Recently a single-arm ultrafast nonlinear interferometer (UNI) gate using an SOA has been demonstrated [10] and this has been shown to be capable of Boolean and up to 100 Gb/s [11].

For the realization of signal processing at ultra high line rates, dual rail logic operations as the Boolean XOR are crucial as they are required to build binary adders [12], data encoders, encryption or comparator circuits. Even though XOR at 100 Gb/s has been demonstrated with the nonlinear loop mirror [13], the highest rate so far with a semiconductor gate is 10 Gb/s [14]. Dual rail logic is harder with semiconductor-based devices, because of the simultaneous presence of two switching pulses that result in deeper saturation of the device. In this letter, we report the demonstration of XOR operation at 20 Gb/s, using the UNI gate with pseudodata control sequences. Low switching energies and low pattern dependence of the switching has been achieved.

II. EXPERIMENT

The concept of operation of the UNI gate relies on polarization rotation of the incoming signal to be switched in the presence of a switching pulse in a SOA [10]. The incoming signal pulse is split into two orthogonal polarization components, which are relatively delayed in a length of birefringent fiber before entry into the SOA. For single logic rail operations, one of these two orthogonal polarizations of the incoming pulse is temporally synchronized with the switching pulse. This causes a local, time-dependent refractive index change in the SOA, which in turn imparts a phase change only on the synchronized polarization component of the signal pulse. On exiting the SOA, the relative delay between the two polarization components of the signal pulses is removed with a fiber of equal birefringence and the pulses are allowed to interfere on a polarizer that determines blocking or transmission through the switch. Long-lived nonlinearities in amplitude and phase are balanced out to first order in the UNI, as they are perceived equally by the two orthogonal polarization components of the signal.

For the implementation of the XOR discussed here, both polarization states of the incoming pulse must be accessed in the SOA with two controlling data pulses. Each controlling pulse imparts a phase and amplitude modulation on the signal polarization component to which it is synchronised. If either controlling pulse is present, the differential phase variation between the orthogonal polarization components results in polarization rotation on the polarizer and the UNI operates as a single rail AND gate. If both controlling pulses are present, the phase change in the orthogonal polarization components may be adjusted to be equal so that no polarization rotation results. In the present experiment three optical signals were used as inputs into the gate. Controls A and B are the logical inputs to the switch and they control its state and CLK is the clock input. The outcome of the logic XOR of A, B is imprinted on CLK, which is held continuously to a logical 1 on input to the gate. Fig. 1 shows the experimental configuration. The three optical signals were produced from two packaged and pigtailed, gain switched DFB semiconductor diode lasers, LD1 and LD2 operating at 1545.2 nm and 1554.6 nm. The laser diodes were driven at 10 GHz from a synthesized RF signal generator and produced 9 ps pulses after linear compression in a dispersion compensating fiber of total dispersion -47 ps/nm. LD1 provided the clock signal CLK and control signal B, while LD2 provided control signal A.

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Fig. 1. Experimental setup.

Different control data patterns have been used for the evaluation of the XOR. For the results shown here, control B was a 10 GHz pulse train and control A was obtained from the 10 GHz pulse train using an LiNbO$_3$ modulator driven from a programmable pulse generator at 625 MHz. The CLK signal from LD1 and the control A from LD2 had their repetition rate doubled, by bit interleaving in a split-relatively-delay-and-recombine fiber doubler. The fiber doubler produced a pseudodata pattern for control A consisting of a 32-bit sequence 00001010101011111111010101010000. Control B was amplified in EDFA 1 while control A and the CLK signals were amplified in EDFA 2 and were subsequently separated for use in the circuit with 2 nm, tunable dielectric filters. The optical power of the control signals was adjusted with attenuators in each signal branch. In the present implementation control pulse trains A and B were brought in counter-propagating direction from the CLK pulse train. Control B pulses were synchronized with the relatively advanced polarization component of the signal pulses and control A with the relatively delayed. The relative delay between control pulses A and B into the SOA was about 25 ps and precise temporal synchronization was effected with optical delay lines ODL A and ODL B.

The input to the UNI gate is a polarization beam splitter (PBS) fiber coupler, with its axes spliced at 45° with the axes of 12 m of polarization maintaining fiber to give 25 ps of relative delay between the two polarization components of the incoming signal pulses. The active switching device was a 1.5-mm long bulk In-GaAsP–InP ridge waveguide type SOA, with its peak small-signal gain of 30 dB at 1558.9 nm when driven with 750-mA current and 80-ps recovery time. Isolators were used at the ports of the SOA to eliminate undesirable reflections in the circuit. The outcoming signal pulses were filtered in a 5-nm filter, had their relative delay removed through propagation in 12 m of birefringent fiber and were made to interfere in a fiber PBS with its axes spliced at 45° with the PM fiber. In the absence of any control pulses the signal appears unswitched in the U port of the

Fig. 2. Logical output for the four logical combinations of control A and B inputs into the gate. The time base is 200 ps/div.

PBS. If either of the control pulses is present, the UNI operates as an AND gate and the signal appears in the switched port S.

III. RESULTS

Successful Boolean XOR operation between A and B is accomplished, when the switched port of the gate records a logical "1" if either A or B is "1" and a logical "0" if both A and B are "1" or "0." Fig. 2 shows the output of the switched port of the gate for four combinations of control data A and B, monitored with a 30-GHz sampling oscilloscope. Bit by bit checking for all logic combinations proves that XOR operation is performed correctly. The operation of the gate was also tested for other control data patterns, including full duty cycle signals and was always found to perform correctly. The contrast ratio between
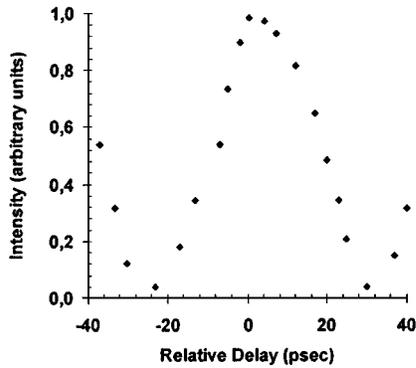
Fig. 3.   Switching window: Dependence of switched port output as arrival time of control B is varied.

the ON–OFF states of the switch was up to 5:1 and the switched signal showed low pattern dependence. It was found that the best switching performance of the gate was obtained for relatively low pulse energy values for the three optical signals, as this ensured lower saturation of the SOA. The energy of the clock, control A and control B pulses was 2, 4, and 10 fJ, respectively. Note that the trailing control pulses A have less energy than the preceding pulses B in order to balance out the heavier gain saturation of the SOA, so that the orthogonal components of CLK signal experience the same gain. These switching energy values are indeed low and the gate may operate in a loss-optimized logic circuit even without an amplifier.

The performance of this logic element in a multi-gate logic circuit will depend on the precision of temporal synchronization of the optical signals and is expected to degrade by timing jitter in the signals. To evaluate this degradation the gate was adjusted for best switching with both controls and the change in the switched bits was recorded as the arrival time of control B was varied with ODL B. Fig. 3 shows the variation of the signal in the switched port of the device. It indicates that the temporal window within which the signal is above its 3-dB value is about 30 ps. This large value of the switching window is in part due to the relatively long pulses used, but nevertheless shows that the device will be tolerant to timing jitter in the incoming data signals.

IV. CONCLUSION

In conclusion, we demonstrate for the first time, to our knowledge, optical Boolean XOR with the Ultrafast Nonlinear Inter-

ferometer gate. Bit pattern switching on 20-Gb/s pseudodata streams was achieved with low pattern dependence, very low-pulse energies and over a wide switching window. In the present experiment the switching rate was limited by the pattern generating laser sources. It is expected that the UNI will be able to perform dual logic operations at significantly higher rates.

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