Architecture, design and physical layer modelling of an all-optical buffering system for all-optical label switched routers

E. Kehayas, L. Stampoulidis, K. Vyrsokinos, D. Apostolopoulos, H. Avramopoulos

Photonics Communications Research Laboratory, National Technical University of Athens,
9 Iroon Polytechniou, Zografou, GR 15773, Greece, E-mail: apostold@mail.ntua.gr

Abstract: We present a new scheme for all-optical contention detection and time-domain contention resolution of optical packets in label-switched routers that employ all-optical label recognition. The contention detection subsystem provides all the necessary control signals required to drive an optically-controlled buffer which employs 1x2 optical switching elements and an optical fiber delay line (FDL). The state of the buffer is dynamically controlled on a per packet basis with all the decisions and processing performed in the optical domain. Physical layer simulations show successful buffering and forwarding of 40 Gb/s optical packets with 2 dB power penalty.

Keywords: Optical packet switching, optical label swapping, buffering, contention resolution, all-optical signal processing, semiconductor optical amplifier.

1. Introduction

Recent advances in communications standards, such as the introduction of Multiprotocol Label Swapping (MPLS) and All-Optical Label Swapping (AOLS) have enabled the integration of the IP layer with the optical layer. In this context, research has been focused on identifying the functionalities required for AOLS and key technologies were developed for their realization [1]. However, three major challenges have haunted the effort towards realizing true AOLS, posing specific requirements on both design and implementation; the lack of functional optical circuit designs, the lack of optical memory elements and the immaturity of photonic integration. Adapting to this reality, AOLS routers have been designed, shifting complex functionalities related to label processing, buffering and contention resolution to the electronic layer [2], [3].

The advances in photonic technology have verified that the realization of functionalities requiring intelligence and processing power directly in the optical domain is not an elusive target. In the case of label processing optical XOR correlation has been a standard all-optical technique designed for employment in a full-scale AOLS system [4], whereas robust, all-optical solutions for on-the-fly contention resolution and buffering have only been presented as stand-alone applications [5-6]. Time-domain contention resolution has been demonstrated only once implementing an all-optical recirculating buffer [6]. Although promising, the technique cannot avoid packet collisions for successive contentions.

In this paper we present a new optical circuit design performing all-optical contention detection and resolution exploiting all-optical signal processing suitable for output-buffered AOLS nodes that employ all-optical label extraction and recognition. All the decisions for forwarding or buffering of optical packets are made on-the-fly by optical gates and memory elements [7]. We validate the feasibility of the design through physical layer simulation using our developed model for a commercially available SOA-Mach-Zehnder interferometric gate (SOA-MZI) [8].

2. Concept

A standard technique to forward optical packets in AOLS nodes [4] is via XOR correlation for label comparison. When a packet enters the AOLS node its label is optically extracted and compared with a number of locally generated labels. The result of this comparison determines on which wavelength and from which output port the packet will exit the node [Fig. 1(a)]. If the result of the label comparison is the same for two different optical packets, these packets will be converted to the same wavelength and sent to the same output port leading to contention [4]. Here we show how this information can be further exploited to realize contention resolution.

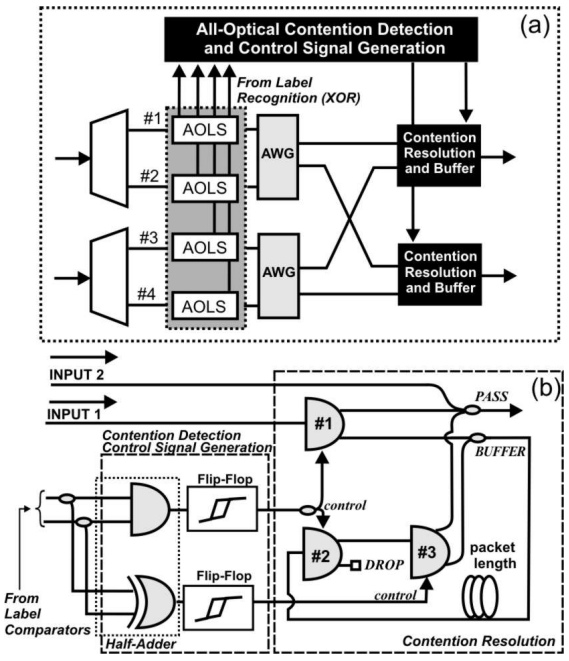

Figure 1 : (a) AOLS node architecture based on optical label processing and internal non-blocking wavelength routing and (b) logical design diagram of all-optical contention detection and resolution.

Figure 1a) shows the logical design of the sub-system. Contention is resolved in two stages; contention is firstly detected with simple all-optical Boolean logic and secondly, this logical result is used to control an all-optical recirculating buffer to sort out the contenting packets. The

contention resolution block consists of a FDL and three optical gates configured to operate as 1x2 switches. Gate #1 is used to deflect the lowest priority packet inside the buffer; Gate #2 decides whether the buffer content should be discarded or not and Gate #3 decides whether a packet should exit the buffer or make another recirculation. Table 1 shows the truth table for the circuit. We note that packet priorities should be first identified based on Class of Service (CoS) information embedded in the packet headers, before forwarding the packets to the correct inputs of the contention resolution block. So, we assume that after packet priorities have been identified, packet #2 enters the contention resolution block from input 2 whereas packet #1 enters from input 1 and packet #3 is the content of the buffer. We also assume that the buffer capacity is equal to one packet.. According to this table, when there is no contention and only one packet appears at the input of the contention resolution block (cases 3-6) the packet is directly forwarded to the output and the content of the buffer remains unchanged. If there are no packets present at the input (case2) the content of the buffer is forwarded to the output. In the case of contention (case 7 and 8) packet #2 is forwarded, the buffer is emptied and packet #1 enters the buffer.

TABLE I
CONTENTION RESOLUTION TRUTH TABLE

Case	P#1 at input 1	P#2 at input 2	P# 3 in Buffer	Pass	Buffer	Drop
1	0	0	0	-	-	-
2	0	0	1	P #3	0	0
3	0	1	0	P #2	0	0
4	0	1	1	P #2	P #3	0
5	1	0	0	P #1	0	0
6	1	0	1	P #1	P #3	0
7	1	1	0	P #2	P #1	0
8	1	1	1	P #2	P #1	P #3

TABLE II
CONTENTION DETECTION TRUTH TABLE

Case	XOR #1	XOR #2	AND	XOR
1	0	0	0	0
2	0	1	0	1
3	1	0	0	1
4	1	1	1	0

To realize these functions the contention detection block should provide the appropriate control signals. Specifically, the contention detection block is an all-optical half-adder (HA), which exploits the information provided by the XOR label comparison of congesting packets whereas optical flip-flops provide the control signals. Table 2 shows the truth table, realizing the following functions:

- Detection of an empty slot (case 1). Both outputs of the HA are '0' and all the 1x2 switches are operated in the switch state forwarding the buffer content to the output.
- Detection of one incoming packet (case 2 and 3). The buffer content is not altered and the incoming packet is forwarded from the input directly to the output. In both cases the XOR result of the HA is '1' and configures gate #3 in the unswitch state forcing the buffer content to re-circulate.
- Detection of collision (case 4). In this case, gate #2 is operated in the unswitch state, dropping the buffer content, packet #2 is forwarded to the output and packet #1 is buffered.

The setup is able to resolve contention for two incoming channels and relies on system cascading for extending to more channels. The scalability of the system, for a NxN AOLS node with N employed wavelengths, i.e. each packet can reach any output only in one wavelength, is Nx(N-1).

3. Simulation Model Development

The complete all-optical system was designed and simulated using a commercially-available simulation tool. We designed the SOA-MZI model to closely match the experimental behavior of the 40 Gb/s 2R regenerator prototypes developed by Center for Integrated Photonics (C.IP. UK) [8]. Fig. 2 shows the comparison between experimental and simulation results. Fig. 2(a) and (b) show static gain measurements of the SOAs within the optical gates, showing good agreement. Fig. 2(c) and (d) show pump-probe measurements for the gain recovery time of the SOAs. Insets show eye diagrams for experimental and simulated 10 Gb/s wavelength conversion. The response time was measured 25 ps and 23 ps at 1/e point, experimentally and by the simulation model respectively.

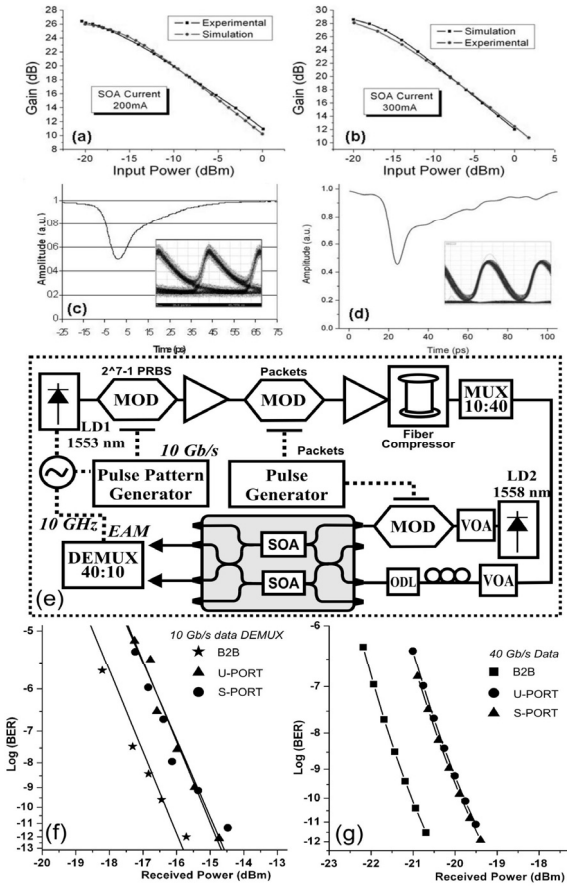

Figure 2 : Comparison between simulation and experimental results. SOA gain response when operated at (a) 200 mA and (b) 300 mA. Recovery time measurements (c) provided by supplier and (d) using the simulation model. Insets show corresponding 10 Gb/s wavelength conversion. Experimental setup (e) and experimental (f) versus simulation (g) BER curves (g) for 40 Gb/s packet switching.

The extinction ratio of the 1x2 optical switches was 15 dB. Fig. 2(e) shows the experimental setup used for comparing experiment and simulation in the case when a single SOA-MZI is gated by a CW packet to switch 40 Gb/s optical packets. Fig. 2(f) and (g) show the experimental and theoretical BER for the 40 Gb/s packets respectively, with the penalties being 1 dB for both S-port and U-port for the experiment and 1.2 dB for the simulation. To reduce the complexity of our model, the control signal generator was modelled as an O/E/O converter followed by a pulse generator.

4. Results and discussion

Fig. 3 shows time-domain results for a contention resolution scenario between two packet streams at 40 Gb/s. Packet stream a) and b) enter the contention resolution block from input2 and input1 respectively, c) is the content of the buffer and d) is the common output of the system. P1 and P4 enter simultaneously the contention resolution block. The AND result of the HA forces gate #1 to operate in the cross state deflecting P4 inside the buffer, whereas P1 appears at the output of the circuit. In the next instance packet P2 appears at one input of the circuit. The AND result of the HA is now '0' and gate #2 is operated in the bar state forwarding P4 to gate #3. The XOR result of the HA being a logical '1' forces gate #3 to operate in the cross state leading to a re-circulation for P4 in the FDL so that P2 can be forwarded to the output without collision. Then two packets appear at both inputs of the circuit. It is the only case where the AND result of the HA is '1' and gate #2 is operated in the cross state dropping P4, as we have assumed a packet length FDL. Then P5 enters the buffer, P3 is forwarded to the output and when an empty time slot is detected, all three gates of the buffer are operated in the bar state so that P5 'fills' the empty slot and appears at the output.

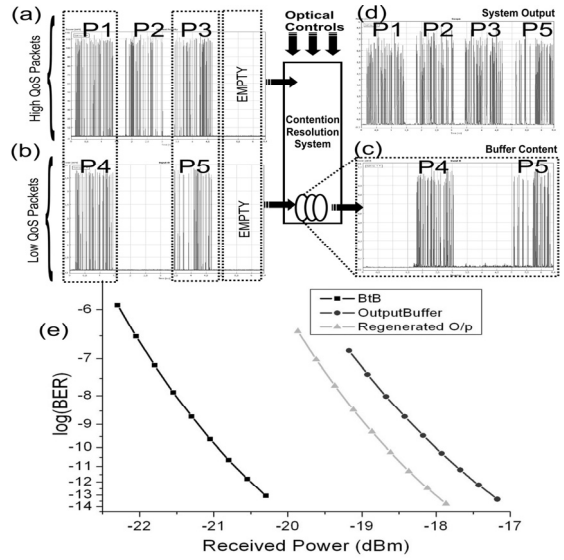

Figure 3 : (a-d) Time-domain traces for the simulated scenario: a) high priority incoming packets, b) low priority incoming packets, c) buffer content and d) output of the system. e) Simulation BER results for back-to-back and output of the system before and after 2R regeneration.

Fig. 3e) shows BER measurements carried out in order to investigate the penalty induced due to packet propagation through the optical buffer. The BER curves correspond to the case where an optical packet has completed two recirculations before exiting the buffer. BER values are estimated through the Q factor. The results show that power penalty of 3 dB was obtained at the output due to OSNR degradation when the packet transverses the cascaded optical gates. This penalty is reduced to 2 dB through 2R regeneration at the output.

TABLE III
BASIC PARAMETERS OF THE SOA-MZI MODEL

Parameter	values	Units
LaserChipLength	1600.0e-06	m
ActiveRegionWidth	1.2e-06	m
ActiveRegionThickness	0.1e-06	m
ConfinementFactor	0.17	
OpticalCouplingEfficiency	0.5	
MaterialLinewidthEnhancementFactor	6	

5. Conclusion

We presented a new design for all-optical contention detection and resolution for AOLS nodes that use optical gates for intelligent processing. The combination of the contention detection and resolution block provides a buffering system that configured on a per packet basis to sort out contenting packets. The system requires only the result of the label comparison to operate, which means that no extra overhead in the labels or control signaling for contention resolution is required.

6. Acknowledgment

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7. References

[1] D. J. Blumenthal: *"Optical Packet Switching"*, ECOC, Stockholm, Sweden, 2004.

[2] D. J. Blumenthal et al.: *"Optical signal processing for optical packet switching networks"*, Communications Magazine, Vol. 41, Issue 2, IEEE, 2003.

[3] Z. Pan et al.: *"Packet-by-Packet wavelength, time, space-domain contention resolution in an Optical-Label Switching router with 2R regeneration"*, Photon. Technol. Lett., Vol. 15, Issue 9, IEEE, 2003.

[4] F. Ramos et al.: *"IST-LASAGNE: Towards All-Optical Label Swapping Employing Optical Logic Gates and Optical Flip-Flops"*, *J. Lightwave Technol.*, Vol. 23, Issue 10, IEEE, 2005.

[5] S. Rangarajan et al.: *"All-Optical Contention Resolution With Wavelength Conversion for Asynchronous Variable-Length 40 Gb/s Optical Packets"*, *Photon. Technol. Lett.*, Vol. 16, Issue 2, IEEE, 2004.

[6] Y. Liu et al.: *"Demonstration of a Variable Optical Delay for a Recirculating Buffer by Using All-Optical Signal Processing"*, Photon. Technol. Lett., Vol. 16, Issue 7, IEEE, 2004.

[7] M. Takenaka, et al.: *"All-Optical Packet Switching by MMI-BLD Optical Flip-Flop."*, OFC, Anaheim, USA, 2006.

[8] G. Maxwell et al.: *"Very low coupling loss, hybrid-integrated all-optical regenerator with passive assembly"*, ECOC, Copenhagen, Denmark, 2002.