

# All-Optical Contention Resolution in Space and Wavelength Domain with Ultra-Fast Packet Envelope Detection and Integrated Optical Gates

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**Abstract** We present a packet-by-packet contention resolution scheme compatible with both NRZ and RZ modulation formats. 10 Gb/s NRZ and 40 Gb/s RZ error-free operation is shown using integrated optical gates.

## Introduction

Contention resolution of optical packets has been identified as one of the most critical functionalities in Optical Label Swapping (OLS) requiring high intelligence and processing power [1]. Research work within this field has focused on unloading such functionalities from the electronic layer directly to the optical domain [2], [3] in order to gain high-speed operation, transparency in data and on-the-fly processing capability offered by all-optical signal processing. However, the penetration of such all-optical systems in next generation optical networks also requires: (1) flexibility in resolving contention in space and wavelength domains, (2) compatibility with modulation formats already used in deployed networks and (3) realization not requiring customized and costly photonic integration solutions.

In this paper we present a new all-optical sub-system performing on-the-fly contention resolution in both space and wavelength domains utilizing generic hybrid integrated gates. The sub-system is capable of operating for both Non-Return and Return-to-Zero (NRZ and RZ) modulation formats by utilizing an all-optical packet envelope detection circuit and additional optical gates for performing deflection and wavelength conversion of contending packets. Error free operation was achieved for 10 Gb/s NRZ and 40 Gb/s RZ packets with power penalties less than 2 dB for both contention resolution strategies.

## Concept and Circuit Design

Fig. 1 shows the schematic diagram of the optical sub-system that is capable of resolving contention in space and wavelength for two incoming packet streams (S1 and S2) that are on the same wavelength. The packet envelope detection (PED) consists of a passive filter in combination with a SOA-MZI optical gate operated as a low-bandwidth 2R regenerator. The PED circuit generates a packet envelope, indicating the presence of a packet at the specific timeslot (P1 in this case). Contention resolution in space is achieved by triggering the 1x2 switch using the PED signals generated by stream S1 to control the packet stream S2. As such, packets of S1 that will contend with packets from S2 are spatially separated (switched) at the optical gate. This packet

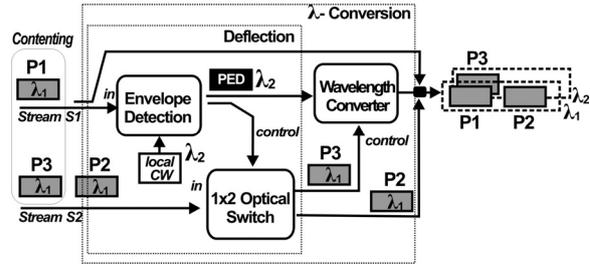


Figure 1. Concept block diagram.

stream can either enter a recirculating buffer or be deflected to a different output port of the node or be wavelength converted, depending on the specific architecture of the label-switched node. In our case, we demonstrate contention resolution in the wavelength domain, using the same PED signal to wavelength convert the deflected packets. In this way, the packets of stream S2 that contend with the packets of stream S1 are wavelength converted onto the packet envelope ( $\lambda_2$ ) generated by stream S1.

## Experimental Setup and Results

Fig. 2(a) and (b) show the two experimental setups, the oscilloscope traces and optical spectra for both 10 Gb/s NRZ and 40Gb/s RZ experiments. For both cases the letters A to F indicate the signals present at different points in the setup. In the NRZ scenario, the traces A and B show the two packet streams entering the contention resolution block. Packet stream B is split into two parts; the first part is connected directly to the output and the second part passes through the PED subsystem, where the envelopes of packets P#4, #5 and #6 are detected (trace/point C). Packet stream A is launched as input in the 1x2 optical switch, which is controlled by the extracted packet envelopes. With this configuration P#1 and P#3 from stream A that coincide temporally with P#4 and P#5 will be deflected by the 1x2 switch (trace D), whereas the separated P#2 (trace E) will be forwarded directly to the output filling the empty slot between P#4 and P#5 (trace F). The deflected P#1 and P#3 enter as control signals in a wavelength converter gated by the detected CW envelopes and the wavelength of these packets is changed (OSA trace F). The operation with 40 Gb/s RZ packets is similar with P#2 and P#4 being the contending packets, whereas P#2 is firstly deflected and then wavelength converted by the

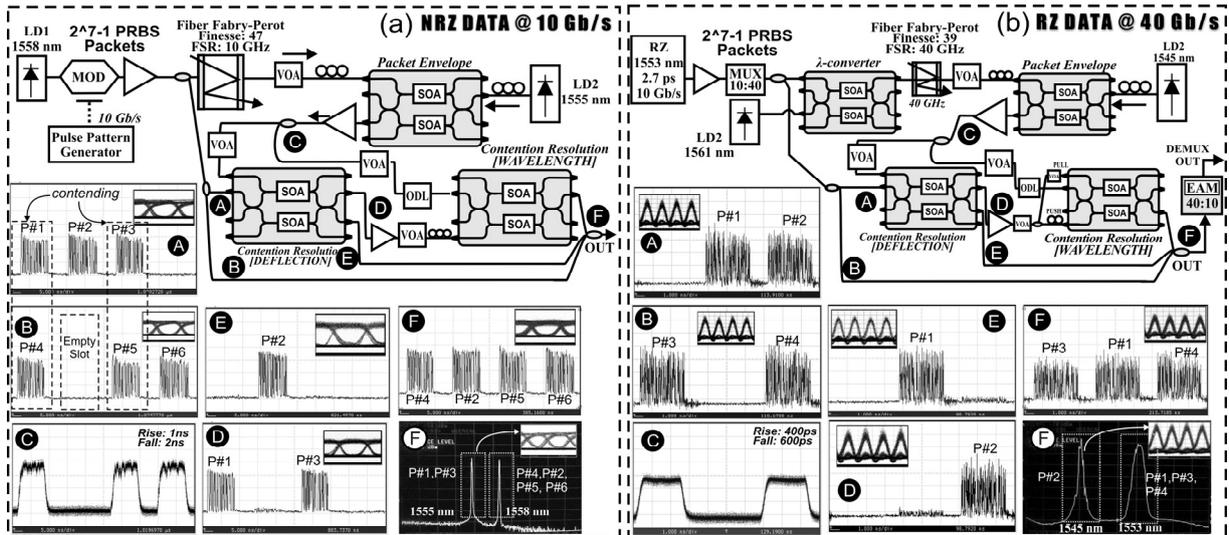


Figure 2. Experimental setup, oscilloscope traces, eye diagrams and optical spectra for (a) 10 Gb/s NRZ and (b) 40 Gb/s RZ operation. Timescales: 5 ns/div and 20 ps/div for the 10 Gb/s NRZ traces and eyes respectively and 1 ns/div and 10 ps/div for the 40 Gb/s RZ traces and eye diagrams respectively.

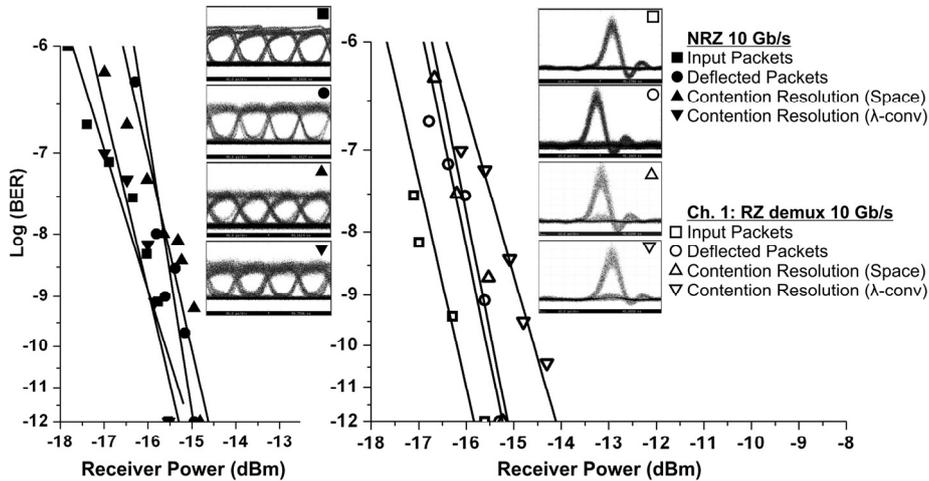


Figure 3. BER measurements and eye diagrams of 10 Gb/s NRZ and 40 Gb/s RZ experiments

envelope of P#4. When no contention occurs, P#1 fills the empty time slot. In both cases the PED circuit employs a Fiber Fabry Perot filter (FFPF) and a saturated optical gate with principle of operation being similar to the one described in [4]. In the case of the 40 Gb/s experiment we employ an additional wavelength converter in a single control configuration before the FFPF to cause pulse broadening and obtain a smooth PED signal. Optical filters of 0.6 nm and 2 nm were used at each gate output for the 10 Gb/s and 40 Gb/s experiments respectively. The complete subsystem was implemented using commercially-available integrated SOA-MZI devices fabricated by C.I.P. UK. Figure 3 shows the BER results for the incoming packets, the deflected packets, the temporally-combined packets and the wavelength converted packets, showing power penalties of less than 1 dB for the 10 Gb/s and less than 2 dB for the 40 Gb/s experiments.

## Conclusions

We have presented on-the-fly contention resolution in

space and wavelength of both RZ and NRZ modulated optical packets. Error-free deflection and wavelength conversion of optical packets is demonstrated, using an all-optical packet envelope detection circuit and optical gates for switching. The complete sub-system was realized using hybrid integrated devices.

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