

# Integrated MZI-based All-Optical Clock and Data Recovery for Asynchronous Variable Packet Length Traffic

D. Tsiokos (1), P. Bakopoulos (1), O. Zouraraki (1), G. Maxwell (2), A. Poustie (2) and H. Avramopoulos (1).

1: Photonics Communications Research Laboratory, National Technical University of Athens

Zographou, GR 15773, Athens, Greece, e-mail: [dtsiokos@mail.ntua.gr](mailto:dtsiokos@mail.ntua.gr)

2: Centre for Integrated Photonics, Adastral Park, Ipswich, IP5 3RE, UK

e-mail: [graeme.maxwell@ciphotonics.com](mailto:graeme.maxwell@ciphotonics.com)

**Abstract** We demonstrate a compact, all-optical, packet Clock and Data Recovery circuit that uses integrated MZIs. Clock is acquired within 2 bits irrespective of packet length and phase alignment. Error-free operation is demonstrated at 10 Gb/s.

## Introduction

Semiconductor-based, all-optical switches have been heavily researched in the past few years [1], primarily due to their integration potential into small footprint matrices. High cost, however, remains a serious stumbling block for market penetration. A major component in the cost of semiconductor optical devices is related to packaging. Research efforts are now underway, for example via the E.C. funded IST project MUFINS, to integrate several Mach-Zehnder Interferometer (MZI) switches on a single chip so as to share the single package costs over them [2]. One clear application for such devices is in receivers for Optical Packet Switched (OPS) networks. OPS traffic arises from several sources and can be assumed to be asynchronous, in the sense that the phase between successive packets is not correlated. In addition, it comprises data packets of variable length and possibly as short as a few hundreds of bytes [3]. Therefore Clock and Data Recovery (CDR) in OPS receivers need to be performed on a per-packet basis with low bandwidth overhead. In CDRs the bandwidth penalty derives from the time that the clock recovery unit needs to acquire clock. As the acquisition time is packet length independent, the bandwidth penalty grows considerably for small packets. All-optical approaches provide the potential for high rate, asynchronous CDR as shown in [4], demonstrating 40 Gb/s operation. Yet, the required locking and essentially the resetting time of this circuit define guardbands comparable to the size of a short IP

packet, still imposing a considerable bandwidth overhead. We have recently demonstrated an ultra-fast locking CDR concept that used a low-Q, Fabry-Pérot etalon resonant at the line rate, followed by two Ultrafast Nonlinear Interferometer gates (UNIs) to obtain the clock packets and corresponding data packets [4]. Even though this design proved the concept, the two polarization maintaining fiber UNI gates made it cumbersome and unwieldy for integration into a small footprint circuit.

In the present communication we show that the CDR concept of [5] can be realized with integrated MZI switches and a Fiber Fabry-Pérot filter (FFP). This results in a compact and stable circuit. The circuit has been evaluated at 10 Gb/s with variable length, synchronous and asynchronous packets. Its acquired clock signal rises 2 bits after packet beginning and falls 15 bits after packet end, resulting in near negligible bandwidth overhead even for short packets. Given that MZI switches have demonstrated operation in the femtosecond regime [6], our CDR could in principle operate at 40 Gb/s and beyond.

## Experiment

The experimental setup consists of the asynchronous, variable length data packet generator and the CDR circuit, comprising the packet clock recovery unit and the decision element, as shown in Fig. 1. A DFB laser diode at 1549.2 nm was gain switched at 10.229 GHz to provide 11 ps pulses after linear compression. This signal was modulated in a lithium niobate modulator to form variable length data packets containing a  $2^7-1$  PRBS data pattern. This pulse train was introduced into a split-and-combine fiber multiplexer, capable of providing up to 12 ns of differential delay between the two paths and controllable asynchronicity between successive packets. Fine phase adjustment was achieved with a variable Optical Delay Line (ODL) positioned in one arm of the multiplexer. Synchronous packet operation could be achieved by disabling one of the branches. The generated packet flow was then injected into the clock recovery unit, consisting of a FFP filter with finesse of 47 and Free Spectral Range (FSR) equal to the line rate, followed by an integrated

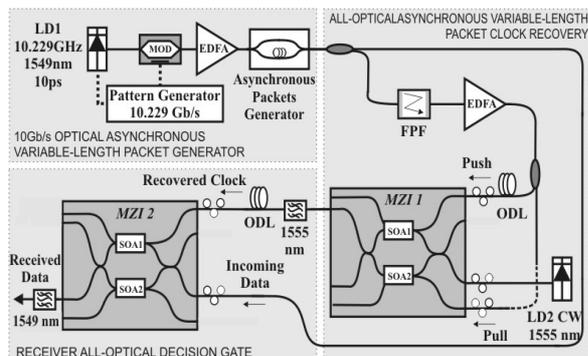


Figure 1: Experimental setup

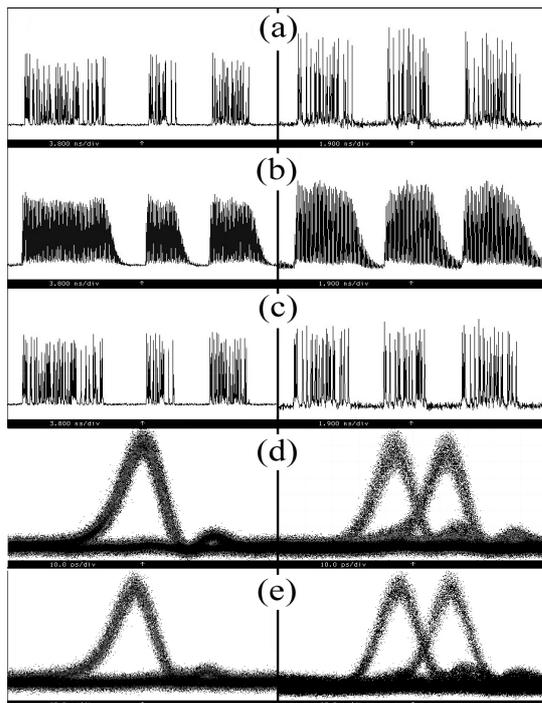


Figure 2: Traces of (a) input, (b) recovered clock, (c) recovered signal (Timescale right: 1.9 ns/div, left: 3.8 ns/div) and eye diagrams of (d) input and (e) recovered signal (timescale: 10 ps/div). Left column: synchronous; right column: asynchronous operation.

Mach-Zehnder Interferometer. The FFP filter acts as a low-Q passive optical resonator that extracts the line rate spectral component of the signal. The data packets are transformed into amplitude-modulated clock packets, as a result of the impulse response of the filter, and provide the control signal for MZI 1. The nonlinear gate operates as a hard limiter saturated by a CW at 1555.6 nm, to equalize the amplitude of the generated clock. This signal samples the input packets at the decision element (MZI 2), performing a logical AND between the data and their corresponding clocks. Both non-linear gates were hybridly integrated MZIs with 1.1 mm SOAs.

## Results

The CDR was evaluated with variable length packet traffic, both synchronous and asynchronous. Typical results are shown in fig 2. The left column of Fig. 2 presents results obtained for synchronous packets, in this instance consisting of 116, 40 and 54 bits. The right hand column shows results for asynchronous packets, in this instance consisting of 40, 30 and 40 bits. Fig. 2(a) shows the input data packets, fig. 2(b) the acquired clock, fig. 2(c) the recovered data packets and fig. 2(d), (e) eye diagrams of input and recovered data signals. Fig. 2(b) shows that the acquired packet clock has a rise time of only 2 bits and a fall time of 15 bits. These time constants are defined by the finesse of the FFP and determine the bandwidth overhead that the CDR imposes.

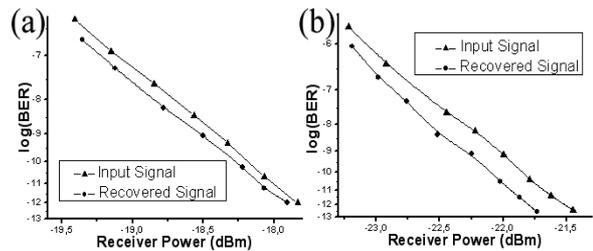


Figure 3: BER measurement for the two packet patterns in synchronous operation

The acquired eye diagrams (Fig. 2 (d)-(e)) reveal a reduction in amplitude and timing jitter owing to the regenerative properties of the circuit. Fig. 3 shows the Bit-Error-Rate performance of the circuit for the two types of packet patterns shown in Fig. 2(a), under synchronous operation. Error-free operation is achieved with negative power penalty. The timing jitter was calculated by integrating the Single Side Band (SSB) noise spectra from offset frequency of 1 kHz to 10 MHz from the carrier, providing root-mean-square (rms) values of 1.3 ps for the input, 700 fs for the clock and 870 fs for the regenerated signal. Amplitude equalization is achieved due to the nonlinear transfer function of the gate, while triggering the input data packets with the self-extracted, low-jitter clock leads to their effective retiming.

The CDR was operationally stable and compact in size, owing to the use of integrated components. The footprint for the MZIs was 72 mm×30 mm and for the FFP filter 57.2 mm×14.3mm. Integration of multiple MZIs on a single chip will decrease size and cost dramatically making a CDR circuit of the present design a realistic choice for OPS network receivers.

## Conclusions

We have presented a compact, all-optical CDR circuit suitable for OPS networks. The overall bandwidth overhead is only 17 bits irrespective of packet length, providing bandwidth efficiency and fine granularity to the network. Compactness, stability and scalability offer the potential to be used in real-life applications.

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## References

- 1 R. Webb et al, ECOC 2002, PD3.5
- 2 <http://mufins.cti.gr/>
- 3 D. J. Blumenthal et al IEEE J. Light. Technol., 18 (2000), 2058.
- 4 J. Slovak et al, ECOC 2004, We.2.5.7, 388.
- 5 G. T. Kanellos et al IEEE Photon. Technol. Letters, 15 (2003), 1666.
- 6 C. K. Yow et al, OFC 2005, OThE4.