

All-Optical SOA-based Packet Detection for Packet-Rate Synchronization

P. Bakopoulos (1), D. Tsiokos (1), D. Apostolopoulos (1), D. Petrantonakis (1), E. Kehayas (1) and H. Avramopoulos (1)

1: Photonics Communications Research Laboratory, National Technical University of Athens, Zographou, GR 15773, Athens, Greece, e-mail: pbakop@mail.ntua.gr

Abstract We demonstrate a simple all-optical technique to detect the beginning of a packet for packet-rate synchronization. It employs a packet clock recovery unit and a SOA and it requires no special data encoding to operate.

Introduction

Optical circuits capable of achieving synchronization at the packet- and bit-level, are critical units for optical signal processors and routers in OTDM networks. The former circuit is essential for packet-level controlling and routing, whereas the latter circuit is required for bitwise signal processing such as 3-R regeneration [1]. Packet-level synchronization can be achieved by extracting the first pulse of the transmitted packet and hence acquiring information on the packet arrival time. Previously reported approaches employ a marker pulse at the beginning of the packet at a different state relative to the rest of the packet, in terms of either wavelength [2], polarization [3], bit period [4] or amplitude [5], resulting in increased complexity to the generation and the transmission of the packets. Recently, experiments have been reported where all the pulses of the packet share the same physical state [6-8]. However in these approaches, a semiconductor optical amplifier (SOA) with very long recovery time is required, introducing long guard bands between the transmitted packets. These circuits also display high pattern dependence requiring strict line coding schemes of the transmitted data [8] and specific packet formats [9].

In the present communication we demonstrate a simple, novel method for all-optical packet-level synchronization at the node processor that requires no marker pulse and operates irrespective of the data and packet format. It employs a clock recovery circuit as reported in [10] and exploits the saturation properties of an additional SOA. The clock recovery circuit consists of a Fabry Perot Filter (FPF) and a SOA-based Ultrafast Non-linear Interferometer (UNI). Following the clock recovery unit, the clock packet is split in two parts that are made to counter-propagate in the SOA with a single bit timing offset. The leftward propagating packet clock is arranged to enter the SOA, one bit in advance of the rightward propagating. Furthermore the power of the two clock packet signals is arranged so that the rightward propagating part provides significantly higher gain saturation than the leftward. In this fashion, we ensure that the leading pulse of the leftward propagating packet clock receives significantly higher gain than the subsequent

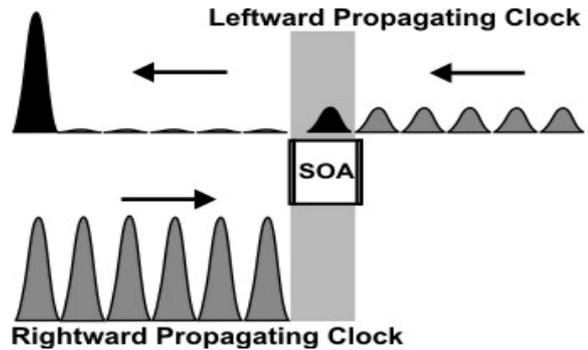


Figure 1: Synchronization of leftward and rightward propagating clock packets in SOA.

packet bits and is discriminated by them. Fig.1 displays graphically the operation of the concept. The proposed circuit was tested with 10 Gb/s pseudorandom data packets and was shown to be highly tolerant to pattern variations. The proposed configuration is simple and can be used as the front-end synchronization sub-system of an optical packet-switched node providing both bit- and packet-level system synchronization, for data regeneration and packet routing respectively.

Experiment

The experimental setup consists of the packet generator, the clock recovery circuit, and the packet-rate pulse generator and is shown in Fig. 2. To generate the data packets, a DFB laser diode (LD1) at 1549nm was gain switched at 2.5815 GHz, providing 10 ps pulses after linear compression. This pulse train was modulated with a 2^7-1 PRBS pattern in a Li:NbO₃ modulator (MOD1) and was inserted in a 2-stage, fiber, bit-interleaver to generate a pseudo-data pattern at 10.326 Gb/s. A second Li:NbO₃ modulator (MOD2), driven by a programmable pulse generator, modulated the PRBS data stream to generate packets of 4 ns length at 80.672 MHz, which then entered the clock recovery circuit. The clock recovery circuit consisted of a FPF with free spectral range (FSR) equal to the line rate and finesse equal to 20.7, followed by a UNI gate [10]. The UNI gate was operated in deep saturation using a counter-propagating CW signal provided by a DFB laser diode (LD2) at 1545 nm forcing the gate to

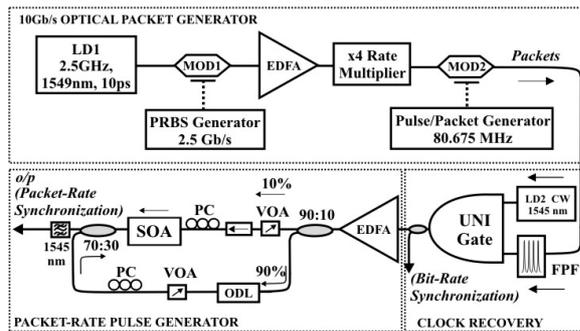


Figure 2: Experimental set-up.

operate as a hard limiter. The active nonlinear element of the gate was a 1.5 mm bulk SOA with 27 dB small signal gain at 1550 nm, and a recovery time of 80 ps, when driven with 700 mA current. After amplification through an EDFA, the extracted clock packets were split and inserted into a 1.5mm SOA in a counter-propagating fashion, synchronized with one bit offset within the amplifier. Variable optical attenuators (VOA) and an optical delay line (ODL) were used to set the respective power and temporal position of the counter propagating signals in the SOA. As drawn in fig. 1, the rightward propagating signal had typical 20 times higher pulse energy and as such it is mainly responsible for SOA saturation. The SOA employed was similar to the device used in the clock recovery circuit, and was also driven with 700 mA current.

Results

The experimental results obtained, are shown in Fig. 3. The left column displays traces for a single packet, while the right column verifies packet-rate synchronization for two consecutive packets. In particular, Fig. 3(a) displays typical data packets entering the circuit while Fig. 3(b) depicts the corresponding recovered clock packets at the output of the clock recovery. The clock displays a sharp lock-in time of two bits, while it falls to $1/e$ within 8 bits. Best operation of the UNI gate was achieved with $900\mu\text{W}$ of CW optical power and 100 fJ/pulse of the data packet signal. The recovered clock packets entered the packet-rate pulse generator which acted as the packet-rate synchronizer by generating a pulse stream with a repetition rate of 80.672 MHz corresponding to the incoming data packet rate. The extinction ratio between the extracted pulse and the suppressed pulses was more than 13 dB. The pulse energies used in the SOA were measured 15 fJ for the leftward propagating signal, and 300 fJ for the rightward propagating signal. The proposed concept introduces short guard bands irrespective of the incoming packet length, and those are defined by the clock recovery circuit. As an example, the total bandwidth overhead of the proposed configuration is 22% for 4 ns incoming packets, while that percentage is reduced to 3% for ATM packets [11].

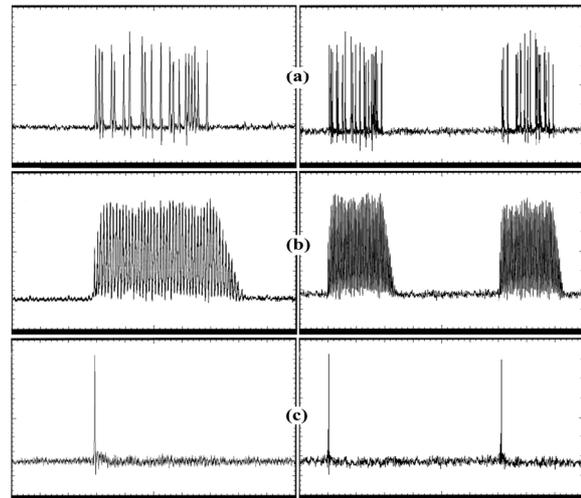


Figure 3: (a) Input data packets, (b) Generated clock packets, (c) Output pulses at packet rate. Left time-base is 1 ns/div and right time-base is 2 ns/div.

Conclusions

We have presented a novel, all-optical circuit that can detect the beginning of optical packets and can be used for packet-rate synchronization. Our technique employs a packet clock recovery circuit and a SOA in a simple configuration. This circuit can in principle operate transparently of packet length with asynchronous or bursty traffic. The circuit imposes short inter-packet guardbands while no special encoding is required in the transmitted data packets. The circuit operation can be extended to 40 Gb/s since the packet synchronizer is independent of the SOA recovery time, while the clock recovery gate, has been demonstrated to operate at 40 GHz [12].

Acknowledgements

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