All-Optical Label/Payload Separation at 40 Gb/s

D. Apostolopoulos, Student Member, IEEE, D. Petrantonakis, O. Zouraraki, Student Member, IEEE, E. Kehayas, Student Member, IEEE, N. Pleros, Member, IEEE, and H. Avramopoulos

Abstract—We demonstrate an all-optical label/payload separation circuit implemented with hybridly integrated semiconductor-optical-amplifier-based Mach–Zehnder switches. It is shown to operate error-free with 40-Gb/s variable length data packets containing $2^7 - 1$ pseudorandom bit sequence and short guardbands between them. The circuit requires only the data packets as input and its complexity does not increase with label length.

Index Terms—All-optical label swapping, integrated Mach–Zehnder interferometer, label separation, optical packet switching.

I. INTRODUCTION

The main concept of all-optical label switching (AOLS) relies on transmitting a short label during the data packet, and on performing all the necessary switching and routing functionalities directly in the optical domain [1]. As such, AOLS networks are expected to offer two main advantages. First, they will release current Internet-protocol-centric nodes from their huge routing tables. The AOLS scenario is compatible with multiprotocol label switching (MPLS) networks and it allows switching to be based on the information contained in the optical label. Second, AOLS networks exploit the inherent fast switching capabilities that their all-optical nature provide and require no optical-to-electrical-to-optical (OEO) conversions with their associated delays [2]. In order to realize AOLS networks, all-optical subsystems must be designed in such a way as not to compromise cost-effectiveness, speed, bandwidth utilization, scalability, and simplicity [3].

A subsystem of crucial importance in a node is the circuit for separating the label from the payload. Its purposes are to forward the label to the label processing unit and the payload to the switching matrix. So far, several label extraction schemes have been proposed including time-to-wavelength mapping [4] and low rate subcarrier multiplexed headers [5]. For efficient bandwidth use, serial label/payload separation concepts have employed self-synchronization techniques [6], [7], different modulation formats for payload and label [8], [9] or keyword address recognition [10]. These solutions have trail blazed implementations of AOLS circuits and underlined the potential of serial all-optical signal processing, their only disadvantage being that their circuit complexity increases with label length and this reduces their scalability.

In this letter, we extend our earlier work [11] and demonstrate, for the first time to our knowledge, a serial label/payload separation circuit based on semiconductor optical amplifier (SOA) Mach–Zehnder interferometric (MZI) switch technology. It has been implemented with three, cascaded, commercially available MZI switches [12] and operates error-free with 40-Gb/s data packets of variable length. It consists of a wavelength converter, a packet clock recovery (CR) unit [13], and an additional MZI switch that performs a logical AND between the input data packet and its properly delayed packet clock. In operation, the circuit requires only the data packet as input, it has low guardband requirements, makes no use of high-speed electronics to perform the label/payload separation, and its complexity does not increase with the label length. Although the circuit is complex, it presents an example of the more sophisticated functionalities that can be obtained with cascades of MZI switches, which are now becoming commercially available in multi-element gate arrays.

II. EXPERIMENTAL SETUP

The experimental setup is shown in Fig. 1. It consists of the 40-Gb/s optical packet generator, the wavelength converter implemented with a hybrid integrated MZI, the packet CR, the label/payload separation unit, and the 40–10-GHz demultiplexer. A 1553-nm distributed feedback laser was gain switched at 10.025 Gb/s to produce 7-ps pulses after linear compression. This pulse train was launched into a nonlinear fiber pulse compressor to reduce its pulsewidth to 3 ps. After exiting the compressor, it passed through a Ti:LiNbO$_3$ electrooptic modulator driven by a 10.025-Gb/s pattern generator and was demultiplexed to 40.1 Gb/s in a fiber bit-interleaver to form data packets containing $2^7 - 1$ pseudorandom bit sequence. The output of the demultiplexer was split and one part was fed as the control signal into the wavelength converter, whereas the other part entered as the input signal to the label/payload separation unit.

The wavelength converter was used in order to locally control the wavelength and the carrier phase of the signal. The new wavelength is used for wavelength conversion and to match one of the transmission peaks of the fiber Fabry–Pérot filter (FFP) employed in the packet CR unit. Controlled carrier phase is also required to assure coherent signal addition in the FFP and the local wavelength converted signal achieves this. The wavelength converter consists of MZI1 operating with push–pull control, and provides at its output a 40-Gb/s data signal at 1545 nm with a pulsewidth of 7 ps. The wavelength converted signal was then amplified and injected into the CR module to achieve all-optical timing extraction. The CR employed a low-$Q$ fiber FFP filter.

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The authors are with the School of Electrical and Computer Engineering, National Technical University of Athens, Zografou, GR 15773 Athens, Greece (e-mail: apostold@mail.ntua.gr).

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with free-spectral range equal to the line rate (40.1 GHz) and a Finesse of 27, followed by MZI2 that was powered by a continuous-wave (CW) signal at 1556 nm (LD2) [13]. The FFP filter transformed each data packet into a clock signal with duration similar to the respective input packet and with intense amplitude modulation. This clock-resembling signal entered the following MZI switch that operates as a power limiter, yielding a power equalized clock packet stream [14]. MZI2 was used with push–pull control configuration to reduce its switching window and to provide 8-ps clock pulses.

The principle of operation of the label extraction process is detailed in Fig. 2(a) and was performed in MZI3 which was configured as an AND gate. The incoming data packet enters in one of the signal ports of MZI3 and its corresponding packet clock enters as control, delayed by a time interval equal to the packet label. In this way, the label bits experience no control signal and exit through the unswitched port (U) of the MZI, while the payload bits exit through its switched port (S) in the presence of the packet clock. Due to the fast but noninstantaneous capture of the CR unit [13], specific guardband bits must be used in the original data packets and Fig. 2(b) shows the packet format adopted. In the examples shown here, the labels had an arbitrarily chosen length of 11 bits with payloads of 71 or 188 bits. The labels included two consecutive “1s” as preamble in their beginning to assist the clock capture. Following the label, a guardband of three consecutive “0s” was used before the payload to avoid inadequate switching by the first pulses of the recovered clock that do not have enough energy. A counterpropagating −14.5-dBm CW signal at 1545 nm provided by LD2 was used in order to saturate the SOAs of MZI3 and to reduce the in-band noise and patterning effect, in this way leading to an extinction ratio improvement by more than 2 dB. The pulsedwidth of both the separated label and payload was 3 ps, equal to the incoming signal’s pulsedwidth, indicating the cascadability potential of the circuit with other node subsystems.

Bit-error-rate (BER) measurements were performed after demultiplexing both the 40-Gb/s packet payloads and the extracted labels into 10-Gb/s data streams using an electroabsorption modulator driven by a 10-GHz signal generator. Short pulses were used in all interferometric switches as input and control signals so as to accommodate the relatively long gain recovery time of the SOAs of the MZI switches. Isolators and polarization controllers were employed between the MZI stages to stop backward propagating noise and signals and to adjust the polarization of the input signals.

### III. RESULTS AND DISCUSSION

Fig. 3 illustrates the evolution of the label/payload separation process through trace and eye diagrams obtained at each stage of the circuit. Fig. 3(a) shows a sequence of two incoming data packets of different length. Fig. 3(b) shows the respective wavelength converted packet stream at the output of the wavelength converter. The incoming packet lengths are 5 and 2.1 ns for the left-hand side and the right-hand side packet, respectively, and the time interval between them is 1.5 ns. Fig. 3(c) shows the recovered clock packets obtained at the output of the CR stage. The recovered clock packets persist for a time equal to the duration of the corresponding data packet extended by 5 and 14 bits at their leading and trailing edges, respectively. The former value corresponds to the time required by the CR to lock to the line-rate of the incoming data packet and is detailed in the inset of Fig. 3(c). The latter value corresponds to the time required by the CR signal to decay to 1/e of its value after each packet. The root-mean-square (rms) jitter of the recovered clock was less than 1 ps, even for rms input data jitter of 4 ps. Fig. 3(d) and (e) shows the separated labels and payloads, obtained at the output of MZI3. Good quality eye diagrams were obtained and the extinction ratio for the extracted label and payload was 9 and 11 dB. Table I summarizes the power/switching energy requirements for the three MZI switches of the circuit.

Fig. 4 shows the BER curves obtained for the four 10-Gb/s label and payload channels at the input, the four 10-Gb/s label channels, and the four 10-Gb/s payload channels at the output of the circuit. Error-free operation was obtained for all demultiplexed channels with a power penalty of up to 1.2 dB for the...
payload channels and 1.8 dB for the label channels with respect to the corresponding input channels, taking into account the power difference between input and output channels. These power penalties are mainly due to the limited extinction ratio of 11 dB for the payload and 9 dB for the label.

IV. CONCLUSION

We have presented an all-optical label/payload separation circuit implemented with a cascade of integrated MZIs. It operates error-free with 40-Gb/s variable length data packets, with short guardbands between them and labels of any, but fixed size. Finally, it is self-synchronizing since it requires only the data packet as input to operate.

REFERENCES


![Fig. 3. Trace and eye diagrams of (a) the incoming data packets, (b) the wavelength converted packets, (c) the packet CR and its rise time, (d) the extracted label, and (e) the extracted payload. The time scale is 1 ns/div for the traces, 200 ps/div for the CR rise time trace, and 10 ps/div for the eye diagrams.](image3)

<table>
<thead>
<tr>
<th>MZI</th>
<th>Input</th>
<th>Control</th>
<th>Push (energy)</th>
<th>Pull (energy)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MZI1 (WC)</td>
<td>7.4 dBm (CW)</td>
<td>61 Ω</td>
<td>15 Ω</td>
<td></td>
</tr>
<tr>
<td>MZI2 (CR)</td>
<td>0 dBm (CW)</td>
<td>700 Ω</td>
<td>300 Ω</td>
<td></td>
</tr>
<tr>
<td>MZI3 (AND)</td>
<td>7 Ω (pulse energy)</td>
<td>37 Ω</td>
<td>-</td>
<td></td>
</tr>
</tbody>
</table>

![Fig. 4. BER measurements.](image4)